DATA SHEET

74LV138

3-to-8 line decoder/multiplexer; inverting

Product specification

IC24 Data Handbook

1997 Feb 03

Philips
Semiconductors

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3-to-8 line decoder/demultiplexer; inverting 74LV138

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV138 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT138.

The 74LV138 accepts three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active LOW outputs ($\overline{Y}_0$ to $\overline{Y}_7$).

The 74LV138 features three enable inputs: two active LOW ($\overline{E}_1$, and $\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the 74LV138 to a 1-of-32 (5 lines to 32 lines) decoder with just four 74LV138 ICs and one inverter. The 74LV138 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state. The 74LV138 is identical to the 74LV238 but has non-inverting (true) outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq$ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to $\overline{Y}n$, E3 to $\overline{Y}n$, $\overline{E}n$ to $\overline{Y}n$	C_L = 15 pF; V_{CC} = 3.3 V	 12 14	 ns ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per package	V_{CC} = 3.3 V V_I = GND to V_{CC}[1]	45	pF

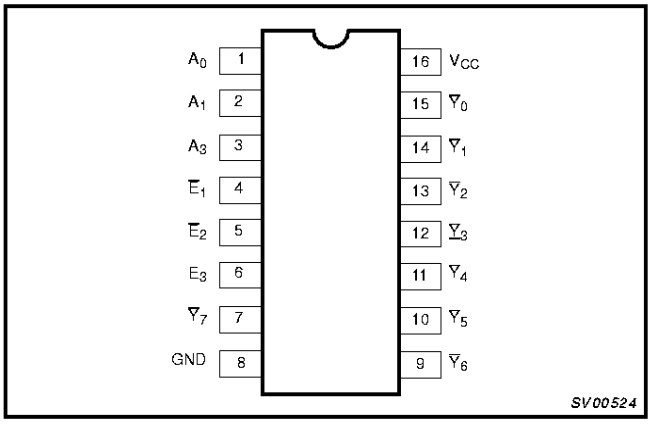
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	−40°C to +125°C	74LV138 N	74LV138 N	SOT38-4
16-Pin Plastic SO	−40°C to +125°C	74LV138 D	74LV138 D	SOT109-1
16-Pin Plastic SSOP Type II	−40°C to +125°C	74LV138 DB	74LV138 DB	SOT338-1
16-Pin Plastic TSSOP Type I	−40°C to +125°C	74LV138 PW	74LV138PW DH	SOT403-1

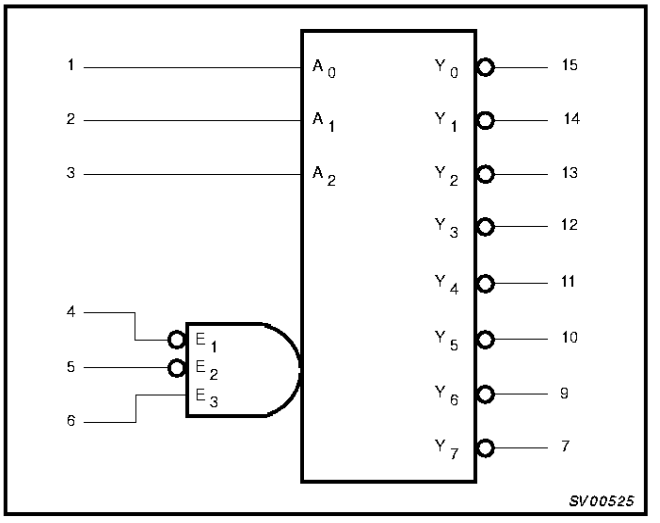
PIN CONFIGURATION



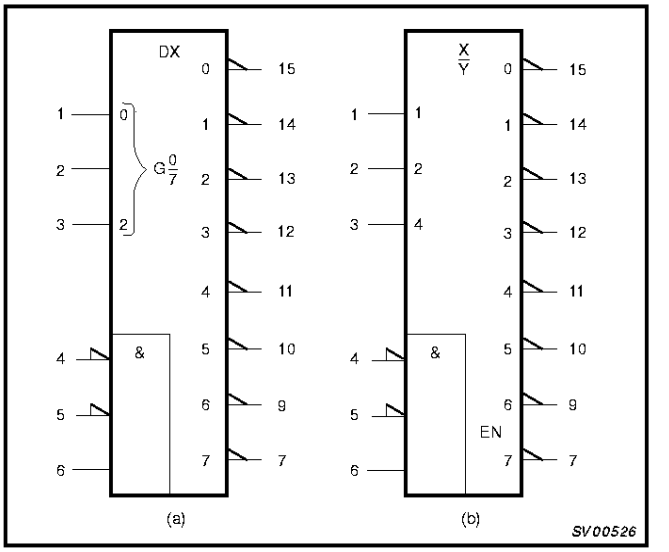
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3	A_0 to A_2	Address inputs
4, 5	$\overline{E}_1$ to $\overline{E}_2$	Enable inputs (active LOW)
6	E_3	Enable inputs (active HIGH)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	Outputs
8	GND	Ground (0 V)
16	V_{CC}	Positive supply voltage

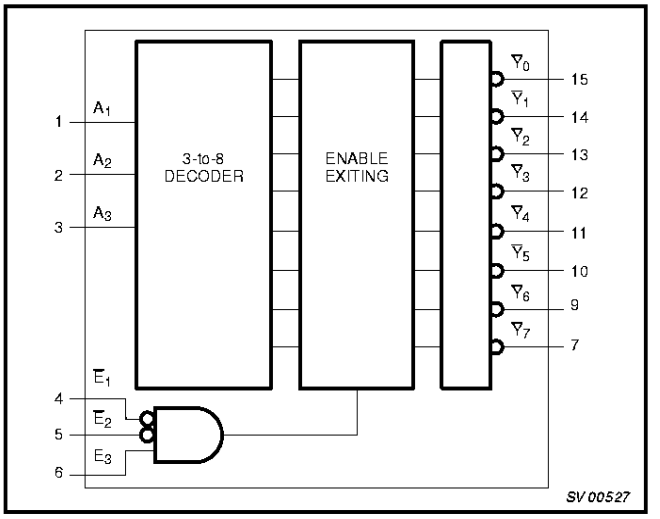
LOGIC DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	 25 35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs – bus driver outputs		 50 70	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics per device	−40 −40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	V_{CC}	0.6		V_{CC}		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
		V_{CC} = 4.5 to 5.5 V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V		0.4	GND		GND	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OH}	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 16mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
V_{OL}	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 8mA		0.20	0.40		0.50	V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 16mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 5.5 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			5		10	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		40	µA
	Quiescent supply current; flip-flops	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		80	
	Quiescent supply current; MSI	V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
	Quiescent supply current; LSI	V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0			500		1000	
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} − 0.6 V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 to +85 °C			−40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay A_n to $\overline{Y}_n$	Figures 1, 3	1.2		75				ns
			2.0		26	36		44	
			2.7		19	26		33	
			3.0 to 3.6		14[2]	21		26	
			4.5 to 5.5		–[3]	16		20	
t_{PHL}/t_{PLH}	Propagation delay E_3 to $\overline{Y}_n$	Figures 1, 3	1.2		85				ns
			2.0		29	39		49	
			2.7		21	29		36	
			3.0 to 3.6		16[2]	23		29	
			4.5 to 5.5		–[3]	19		24	
t_{PHL}/t_{PLH}	Propagation delay $\overline{E}_n$ to $\overline{Y}_n$	Figures 2, 3	1.2		85				ns
			2.0		29	39		49	
			2.7		21	29		36	
			3.0 to 3.6		16[2]	23		29	
			4.5 to 5.5		–[3]	19		24	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.
3. Typical values are measured at V_{CC} = 5.0 V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V and ≤ 3.6 V;
V_M = 0.5 V × V_{CC} at V_{CC} < 2.7 V and ≥ 4.5 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

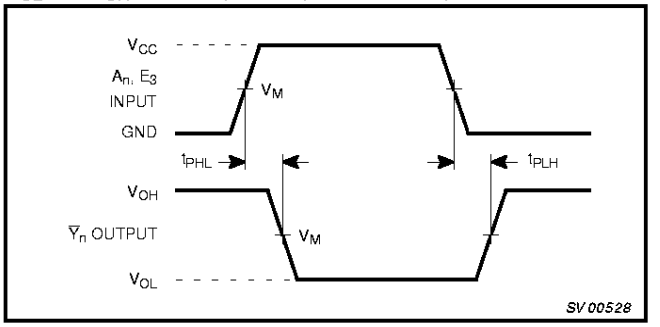


Figure 1. Input (An) and enable input (E_3) to output ($\overline{Y}n$) propagation delays.

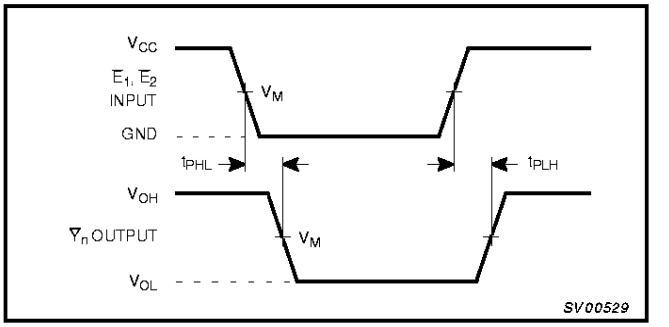
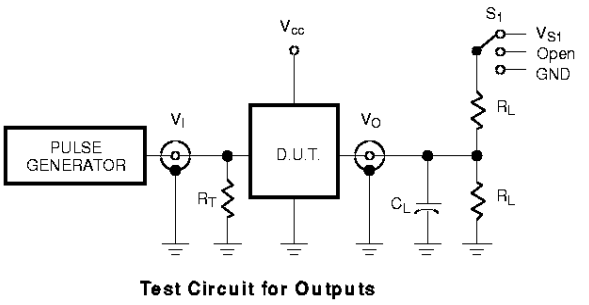
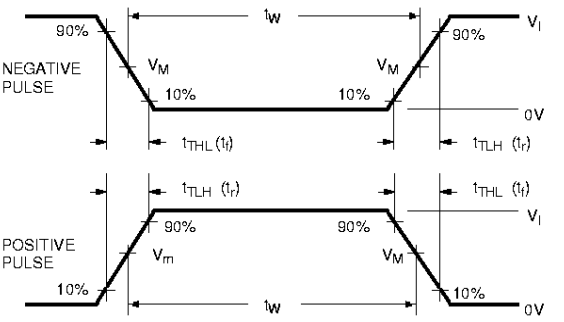


Figure 2. Enable input ($\overline{E}_n$) to output ($\overline{Y}n$) propagation delays.

TEST CIRCUIT



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{S1}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I	V_{S1}
< 2.7V	V_{CC}	2 * V_{CC}
2.7–3.6V	2.7V	2 * V_{CC}
≥ 4.5 V	V_{CC}	2 * V_{CC}

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SY00044

Figure 3. Load circuitry for switching times.

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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