

# TYPES SN54ALS874, SN54ALS876, SN54AS874, SN54AS876 SN74ALS874, SN74ALS876, SN74AS874, SN74AS876 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

D2661, APRIL 1982—REVISED DECEMBER 1983

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Choice of True or Inverting Logic
  - 'ALS874, 'AS874 True Outputs
  - 'ALS876, 'AS876 Inverting Outputs
- Asynchronous Clear
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

## description

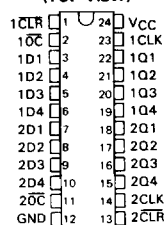
These dual four-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The edge-triggered flip-flops enter data on the low-to-high transition of the clock. The 'ALS874 and 'AS874 have  $\overline{\text{CLR}}$  inputs and noninverting Q outputs; the 'ALS876 and 'AS876 have PRE inputs and inverting  $\overline{\text{Q}}$  outputs. In each case, taking this input low causes the four Q or  $\overline{\text{Q}}$  outputs to go low independently of the clock.

The SN54ALS874, SN54AS874, SN54ALS876 and SN54AS876 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS874, SN74AS874, SN74ALS876, and SN74AS876 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

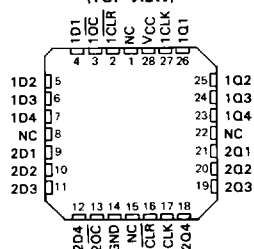
SN54ALS874, SN54AS874 . . . JT PACKAGE  
SN74ALS874, SN74AS874 . . . NT PACKAGE

(TOP VIEW)



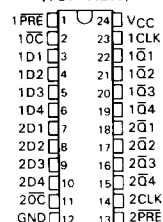
SN54ALS874, SN54AS874 . . . FH PACKAGE  
SN74ALS874, SN74AS874 . . . FN PACKAGE

(TOP VIEW)



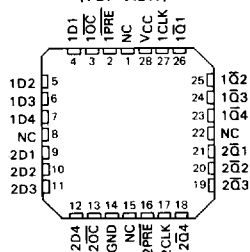
SN54ALS876, SN54AS876 . . . JT PACKAGE  
SN74ALS876, SN74AS876 . . . NT PACKAGE

(TOP VIEW)



SN54ALS876, SN54AS876 . . . FH PACKAGE  
SN74ALS876, SN74AS876 . . . FN PACKAGE

(TOP VIEW)



NC — No internal connection

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ALS AND AS CIRCUITS

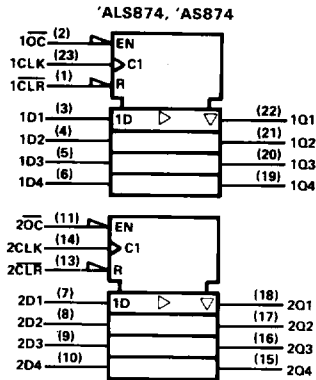
**TYPES SN54ALS874, SN54ALS876, SN54AS874, SN54AS876  
SN74ALS874, SN74ALS876, SN74AS874, SN74AS876  
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

FUNCTION TABLES

'ALS874, 'AS874 (EACH FLIP-FLOP)

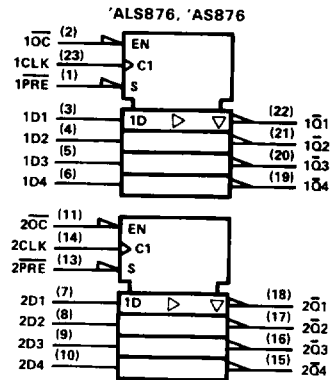
INPUTS				OUTPUT
$\overline{OC}$	CLR	CLK	D	Q
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	$Q_0$
H	X	X	X	Z

logic symbols



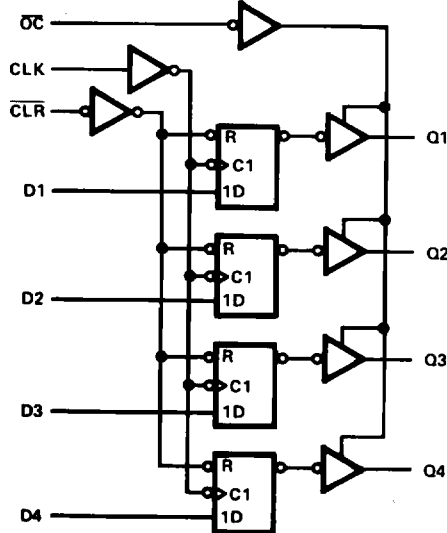
'ALS876, 'AS876 (EACH FLIP-FLOP)

INPUTS				OUTPUT
$\overline{OC}$	PRE	CLK	D	$\overline{Q}$
L	L	X	X	L
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

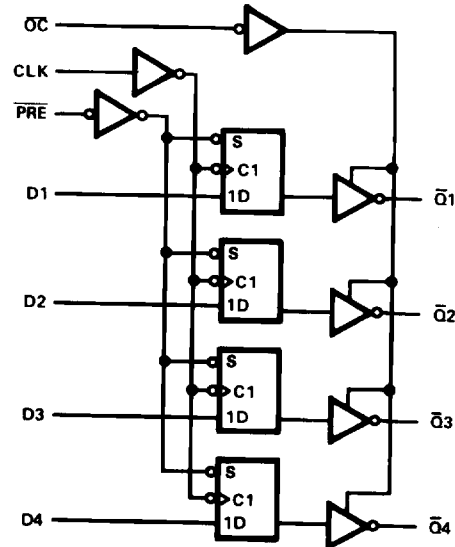


logic diagrams (positive logic)

'ALS874, 'AS874 (EACH QUAD FLIP-FLOP)



'ALS876, 'AS876 (EACH QUAD FLIP-FLOP)



Pin numbers shown are for JT and NT packages.

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ALS AND AS CIRCUITS

**TYPES SN54ALS874, SN54ALS876  
SN74ALS874, SN74ALS876  
DUAL 4-BIT D-TYPE EDGE-TRIGGERD FLIP-FLOPS**

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ .....	7 V
Input voltage .....	7 V
Voltage applied to a disabled 3-state output .....	5.5 V
Operating free-air temperature range: SN54ALS874, SN54ALS876 .....	-55 °C to 125 °C
SN74ALS874, SN74ALS876 .....	0 °C to 70 °C
Storage temperature range .....	-65 °C to 150 °C

**recommended operating conditions**

		SN54ALS874 SN54ALS876			SN74ALS874 SN74ALS876			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage	0.8			0.8			V
$I_{OH}$	High-level output current	-1			-2.6			mA
$I_{OL}$	Low-level output current	12			24			mA
$f_{clock}$	Clock frequency	0		25	0		30	MHz
$t_w$	Pulse duration	PRE or CLR low		10	10		ns	
		CLK high		20	16.5			
		CLK low		20	16.5			
$t_{su}$	Setup time before CLK †	Data		15	15		ns	
		PRE or CLR inactive		10	10			
$t_h$	Hold time, data after CLK †	4		0		ns		
$T_A$	Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54ALS874 SN54ALS876		SN74ALS874 SN74ALS876		UNIT		
		MIN	TYP †	MAX	MIN		TYP †	MAX
$V_{IK}$	$V_{CC} = 4.5 V, I_I = -18 mA$			-1.5		V		
$V_{OH}$	$V_{CC} = 4.5 V \text{ to } 5.5 V, I_{OH} = -0.4 mA$	$V_{CC} - 2$		$V_{CC} - 2$		V		
	$V_{CC} = 4.5 V, I_{OH} = -1 mA$	2.4	3.3					
	$V_{CC} = 4.5 V, I_{OH} = -2.6 mA$			2.4	3.2			
$V_{OL}$	$V_{CC} = 4.5 V, I_{OL} = 12 mA$	0.25		0.4	0.25	0.4	V	
	$V_{CC} = 4.5 V, I_{OL} = 24 mA$			0.35		0.5		
$I_{OZH}$	$V_{CC} = 5.5 V, V_O = 2.7 V$			20		μA		
$I_{OZL}$	$V_{CC} = 5.5 V, V_O = 0.4 V$			-20		μA		
$I_I$	$V_{CC} = 5.5 V, V_I = 7 V$			0.1		mA		
$I_{IH}$	$V_{CC} = 5.5 V, V_I = 2.7 V$			20		μA		
$I_{IL}$	$V_{CC} = 5.5 V, V_I = 0.4 V$			-0.2		mA		
$I_O ‡$	$V_{CC} = 5.5 V, V_O = 2.25 V$	-15		-70	-15		-70	mA
$I_{CC}$	$V_{CC} = 5.5 V$	Outputs high		14	21		mA	
		Outputs low		18	29			
		Outputs disabled		20	31			

† All typical values are at  $V_{CC} = 5 V, T_A = 25 °C$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

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**ALS AND AS CIRCUITS**

**TYPES SN54ALS874, SN54ALS876  
SN74ALS874, SN74ALS876  
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

**\*ALS874 switching characteristics (see Note 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54ALS874		SN74ALS874		
			MIN	MAX	MIN	MAX	
$f_{\text{max}}$			25		30		MHz
$t_{\text{PLH}}$	CLK	Any Q	4	15	4	14	ns
$t_{\text{PHL}}$			4	15	4	14	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Any Q	6	22	6	19	ns
$t_{\text{PZH}}$	$\overline{\text{OC}}$	Any Q	4	21	4	18	ns
$t_{\text{PZL}}$			4	21	4	18	
$t_{\text{PHZ}}$	$\overline{\text{OC}}$	Any Q	2	10	2	8	ns
$t_{\text{PLZ}}$			3	15	3	13	

**\*ALS876 switching characteristics (see Note 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54ALS876		SN74ALS876		
			MIN	MAX	MIN	MAX	
$f_{\text{max}}$			25		30		MHz
$t_{\text{PLH}}$	CLK	Any $\overline{\text{Q}}$	4	15	4	14	ns
$t_{\text{PHL}}$			4	15	4	14	
$t_{\text{PHL}}$	$\overline{\text{PRE}}$	Any $\overline{\text{Q}}$	6	22	6	19	ns
$t_{\text{PZH}}$	$\overline{\text{OC}}$	Any $\overline{\text{Q}}$	4	21	4	18	ns
$t_{\text{PZL}}$			4	21	4	18	
$t_{\text{PHZ}}$	$\overline{\text{OC}}$	Any $\overline{\text{Q}}$	2	10	2	8	ns
$t_{\text{PLZ}}$			3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

## TYPES SN54AS874, SN54AS876, SN74AS874, SN74AS876 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ .....	7 V
Input voltage .....	7 V
Operating free-air temperature range: SN54AS874, SN54AS876 .....	-55 °C to 125 °C
SN74AS874, SN74AS876 .....	0 °C to 70 °C
Storage temperature range .....	-65 °C to 150 °C

recommended operating conditions

		SN54AS874 SN54AS876			SN74AS874 SN74AS876			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage				0.8			V
$I_{OH}$	High-level output current				-12			mA
$I_{OL}$	Low-level output current				32			mA
$f_{clock}$	Clock frequency	0		100	0		125	MHz
$t_w$	Pulse duration	PRE or CLR low		3	2		ns	
		CLK high		4	3			
		CLK low		5	4			
$t_{su}$	Setup time before CLK ↑	Data		2.5	2		ns	
		PRE or CLR inactive		5	4			
$t_h$	Hold time, data after CLK ↑	1		1	1		ns	
$T_A$	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS874 SN54AS876			SN74AS874 SN74AS876			UNIT
		MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	
$V_{IK}$	$V_{CC} = 4.5 V, I_I = -18 mA$	-1.2			-1.2			V
$V_{OH}$	$V_{CC} = 4.5 V \text{ to } 5.5 V, I_{OH} = -2 mA$	$V_{CC} - 2$		$V_{CC} - 2$	$V_{CC} - 2$			V
	$V_{CC} = 4.5 V, I_{OH} = -12 mA$	2.4	3.2					
	$V_{CC} = 4.5 V, I_{OH} = -15 mA$			2.4	3.3			
$V_{OL}$	$V_{CC} = 4.5 V, I_{OL} = 32 mA$	0.25	0.5				V	
	$V_{CC} = 4.5 V, I_{OL} = 48 mA$			0.35	0.5			
$I_{OZH}$	$V_{CC} = 5.5 V, V_O = 2.7 V$	50			50			μA
$I_{OZL}$	$V_{CC} = 5.5 V, V_O = 0.4 V$	-50			-50			μA
$I_I$	$V_{CC} = 5.5 V, V_I = 7 V$	0.1			0.1			mA
$I_{IH}$	$V_{CC} = 5.5 V, V_I = 2.7 V$	20			20			μA
$I_{IL}$	$V_{CC} = 5.5 V, V_I = 0.4 V$	D		-3	-2		mA	
		All other		-0.5	-0.5			
$I_O^{\ddagger}$	$V_{CC} = 5.5 V, V_O = 2.25 V$	-30	-112	-30	-112	mA		
$I_{CC}$	$V_{CC} = 5.5 V$		Outputs high	82	133	82	133	mA
			Outputs low	92	149	92	149	
			Outputs disabled	100	160	100	160	
			Outputs high	88	142	88	142	
			Outputs low	94	150	94	150	
			Outputs disabled	100	160	100	160	

<sup>†</sup>All typical values are at  $V_{CC} = 5 V, T_A = 25 °C$ .

<sup>‡</sup>The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

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ALS AND AS CIRCUITS

**TYPES SN54AS874, SN54AS876, SN74AS874, SN74AS876**  
**DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

**'AS874 switching characteristics (see Note 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS874		SN74AS874		
			MIN	MAX	MIN	MAX	
$f_{\max}$			100		125		MHz
$t_{PLH}$	CLK	Any Q	3	11.5	3	8.5	ns
$t_{PHL}$			4	12.5	4	10.5	
$t_{PHL}$	CLR	Any Q	4	11	4	9.5	ns
$t_{PZH}$	OC	Any Q	2	8	2	7	ns
$t_{PZL}$			3	11.5	3	10.5	
$t_{PHZ}$	OC	Any Q	2	7	2	6	ns
$t_{PLZ}$			2	8.5	2	7.5	

**'AS876 switching characteristics (see Note 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS876		SN74AS876		
			MIN	MAX	MIN	MAX	
$f_{\max}$			100		125		MHz
$t_{PLH}$	CLK	Any $\bar{Q}$	3	11.5	3	8.5	ns
$t_{PHL}$			4	12.5	4	10.5	
$t_{PHL}$	PRE	Any $\bar{Q}$	4	11	4	9.5	ns
$t_{PZH}$	OC	Any $\bar{Q}$	2	8	2	7	ns
$t_{PZL}$			3	11.5	3	10.5	
$t_{PHZ}$	OC	Any $\bar{Q}$	2	7	2	6	ns
$t_{PLZ}$			2	7	2	6	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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**ALS AND AS CIRCUITS**