

54AC/74AC823 • 54ACT/74ACT823 54AC/74AC824 • 54ACT/74ACT824

9-Bit D-Type Flip-Flop

Description

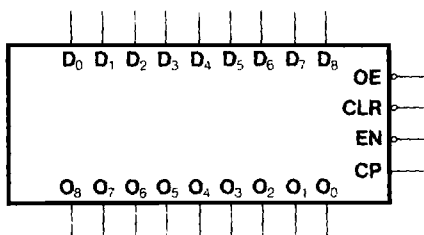
The 'AC/'ACT823 and 'AC/'ACT824 are 9-bit buffered registers. They feature Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems. The 'AC/'ACT 823 offers noninverting outputs and the 'AC/'ACT824 offers inverting outputs.

The 'AC/'ACT823 is fully compatible with AMD's AM29823.

- **Outputs Source/Sink 24 mA**
- **3-State Outputs for Bus Interfacing**
- **Inputs and Outputs are on Opposite Sides**
- **'ACT823 and 'ACT824 have TTL-Compatible Inputs**

Ordering Code: See Section 6

Logic Symbol ('AC/'ACT823)*

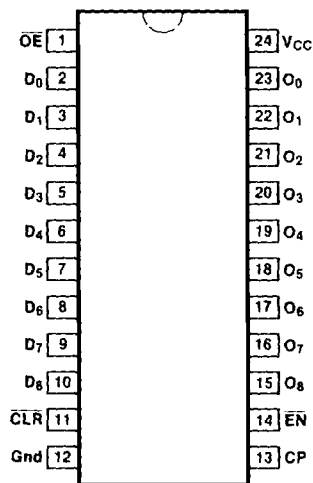


*The 'AC/'ACT824 has inverting outputs.

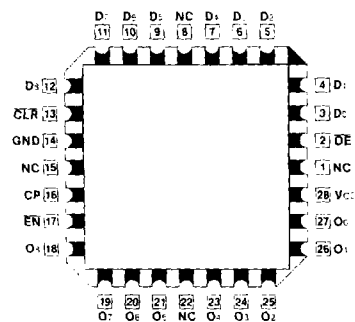
Pin Names

$D_0 - D_8$	Data Inputs
$O_0 - O_8$	Data Outputs ('AC/'ACT823)
$\bar{O}_0 - \bar{O}_8$	Data Outputs ('AC/'ACT824)
\bar{OE}	Output Enable
\bar{CLR}	Clear
CP	Clock Input
EN	Clock Enable

Connection Diagrams



**Pin Assignment
for DIP, Flatpak and SOIC**



**Pin Assignment
for LCC**

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Functional Description

The 'AC'/ACT823 and 'AC'/ACT824 consist of nine D-type edge-triggered flip-flops. These have 3-state outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable (\overline{OE}) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With \overline{OE} LOW, the contents of the flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect

the state of the flip-flops. In addition to the Clock and Output Enable pins, there are Clear (\overline{CLR}) and Clock Enable (\overline{EN}) pins. These devices are ideal for parity bus interfacing in high performance systems.

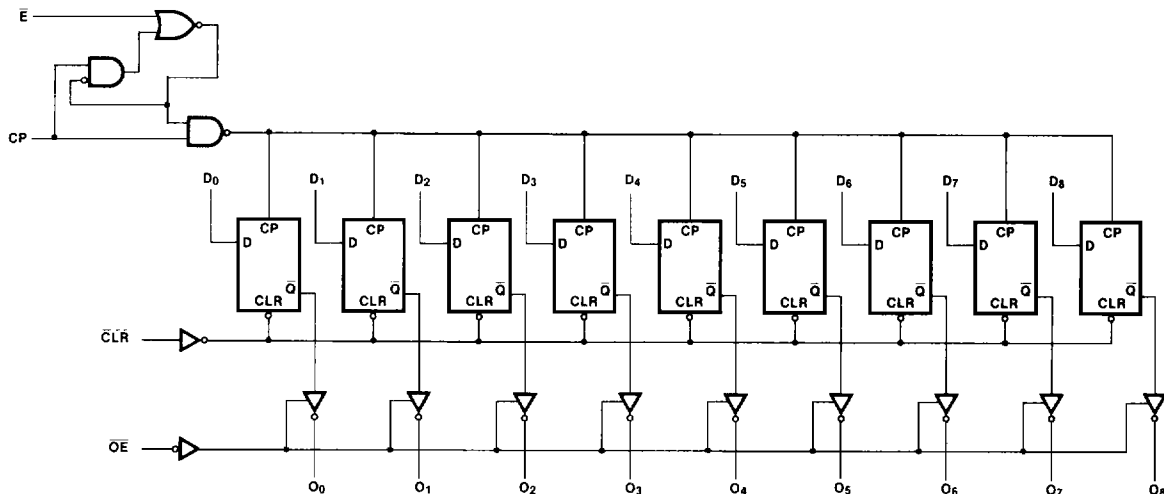
When \overline{CLR} is LOW and \overline{OE} is LOW, the outputs are LOW. When \overline{CLR} is HIGH, data can be entered into the flip-flops. When \overline{EN} is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the \overline{EN} is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Outputs		Function
\overline{OE}	\overline{CLR}	\overline{EN}	CP	D	Q	O ('823)	\overline{O} ('824)	
H	X	L	J	L	L	Z	Z	High Z
H	X	L	J	H	H	Z	Z	High Z
H	L	X	X	X	L	Z	Z	Clear
L	L	X	X	X	L	L	L	Clear
H	H	H	X	X	NC	Z	Z	Hold
L	H	H	X	X	NC	NC	NC	Hold
H	H	L	J	L	L	Z	Z	Load
H	H	L	J	H	H	Z	Z	Load
L	H	L	J	L	L	L	H	Load
L	H	L	J	H	H	H	L	Load

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 J = LOW-to-HIGH Transition
 NC = No Change

Logic Diagram ('AC/ACT823)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The 'AC/ACT824 also has the same logic diagram with inverting outputs.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 \text{ V}$, $T_A = \text{Worst Case}$
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 \text{ V}$, $T_A = 25^\circ\text{C}$
I_{CCT}	Maximum Additional I_{CC} /Input ('ACT823/824)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1 \text{ V}$ $V_{CC} = 5.5 \text{ V}$, $T_A = \text{Worst Case}$

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC			54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
fmax	Maximum Clock Frequency	3.3 5.0		100 125					MHz	3-3	
tPLH	Propagation Delay CP to On	3.3 5.0		9.5 6.5					ns	3-6	
tPHL	Propagation Delay CP to On	3.3 5.0		9.5 6.5					ns	3-6	
tPHL	Propagation Delay CLR to On	3.3 5.0		14.5 10.5					ns	3-6	
tpZH	Output Enable Time OE to On	3.3 5.0		7.5 5.5					ns	3-7	
tpZL	Output Enable Time OE to On	3.3 5.0		8.0 6.0					ns	3-8	
tPHZ	Output Disable Time OE to On	3.3 5.0		10.5 7.5					ns	3-7	
tPLZ	Output Disable Time OE to On	3.3 5.0		8.5 6.0					ns	3-8	

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC		54AC	74AC	Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF		
			Typ	Guaranteed Minimum				
ts	Setup Time, HIGH or LOW Dn to CP	3.3 5.0	3.0 2.0				ns	3-9
th	Hold Time, HIGH or LOW Dn to CP	3.3 5.0	2.0 1.5				ns	3-9
ts	Setup Time, HIGH or LOW EN to CP	3.3 5.0	3.0 2.0				ns	3-9
th	Hold Time, HIGH or LOW EN to CP	3.3 5.0	2.0 1.5				ns	3-9
tw	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5				ns	3-6
tw	CLR Pulse Width, LOW	3.3 5.0	5.0 3.5				ns	3-6
trec	CLR to CP Recovery Time	3.3 5.0	2.0 1.5				ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
fmax	Maximum Clock Frequency	5.0	110							MHz	3-3
tPLH	Propagation Delay CP to On	5.0	8.0							ns	3-6
tPHL	Propagation Delay CP to On	5.0	8.0							ns	3-6
tPHL	Propagation Delay CLR to On	5.0	12.0							ns	3-6
tPZH	Output Enable Time OE to On	5.0	7.0							ns	3-7
tPZL	Output Enable Time OE to On	5.0	7.5							ns	3-8
tPHZ	Output Disable Time OE to On	5.0	10.0							ns	3-7
tPLZ	Output Disable Time OE to On	5.0	8.5							ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	V _{CC} * (V)	74ACT		54ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum						
t _s	Setup Time, HIGH or LOW D to CP	5.0	2.0						ns	3-9
t _h	Hold Time, HIGH or LOW D _n to CP	5.0	1.0						ns	3-9
t _s	Setup Time, HIGH or LOW EN to CP	5.0	2.0						ns	3-9
t _h	Hold Time, HIGH or LOW EN to CP	5.0	1.5						ns	3-9
t _w	CP Pulse Width HIGH or LOW	5.0	3.0						ns	3-6
t _w	CLR Pulse Width, LOW	5.0	4.0						ns	3-6
t _{rec}	CLR to CP Recovery Time	5.0	1.5						ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.5 V
C _{PD}	Power Dissipation Capacitance		pF	V _{CC} = 5.5 V