

**Features**

- $I_{off}$  supports partial-power-down mode operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$

*CY74FCT16240T Features:*

- 64 mA sink current, 32 mA source current
- Typical  $V_{OLP}$  (ground bounce) < 1.0V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

*CY74FCT162240T Features:*

- Balanced output drivers: 24 mA
- Reduced system switching noise
- Typical  $V_{OLP}$  (ground bounce) < 0.6V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

**Functional Description**

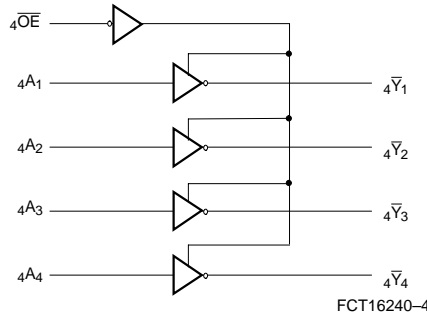
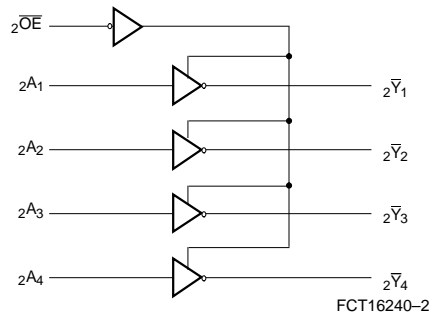
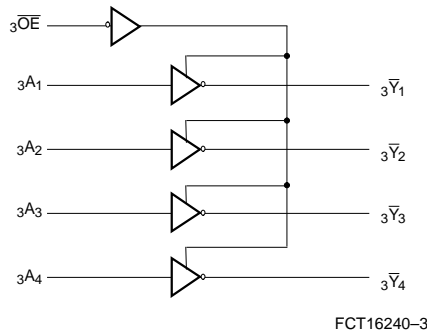
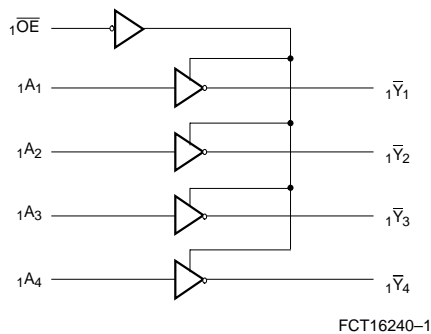
These 16-bit buffer/line drivers are used in memory driver, clock driver, or other bus interface applications, where high speed and low power are required. With flow-through pinout and small shrink packaging, board layout is simplified. The three-state controls are designed to allow 4-, 8-, or 16-bit operation.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

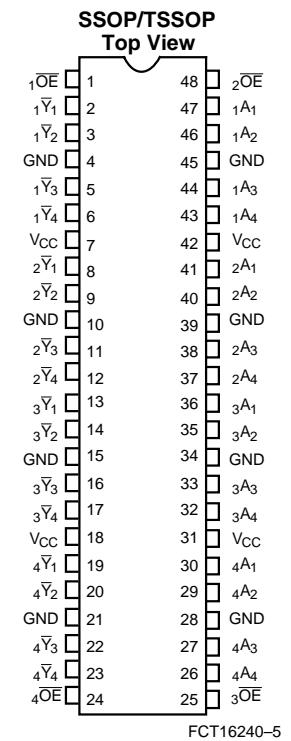
The CY74FCT16240T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162240T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162240T is ideal for driving transmission lines.

**Logic Block Diagrams**



**Pin Configuration**



**Pin Summary**

Name	Description
$\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
A	Data Inputs
$\overline{Y}$	Three-State Outputs

**Function Table<sup>[1]</sup>**

Inputs		Outputs
$\overline{OE}$	A	$\overline{Y}$
L	L	H
L	H	L
H	X	Z

**Maximum Ratings<sup>[2, 3]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....Com'l. -55°C to +125°C

Ambient Temperature with Power Applied.....Com'l. -55°C to +125°C

DC Input Voltage ..... -0.5V to +7.0V

DC Output Voltage..... -0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....-60 to +120 mA

Power Dissipation ..... 1.0W

Static Discharge Voltage (per MIL-STD-883, Method 3015) .....>2001V

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>IL</sub>	Input LOW Voltage				0.8	V
V <sub>H</sub>	Input Hysteresis <sup>[5]</sup>			100		mV
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA		-0.7	-1.2	V
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>I</sub> = V <sub>CC</sub>			±1	µA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>I</sub> = V <sub>CC</sub>			±1	µA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>I</sub> = GND			±1	µA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>I</sub> = GND			±1	µA
I <sub>OZH</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 2.7V			±1	µA
I <sub>OZL</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V			±1	µA
I <sub>OS</sub>	Short Circuit Current <sup>[6]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND	-80	-140	-200	mA
I <sub>O</sub>	Output Drive Current <sup>[6]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 2.5V	-50		-180	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> = 0V, V <sub>OUT</sub> ≤ 4.5V <sup>[7]</sup>			±1	µA

**Output Drive Characteristics for CY74FCT16240T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -3 mA	2.5	3.5		V
		V <sub>CC</sub> = Min., I <sub>OH</sub> = -15 mA	2.4	3.5		V
		V <sub>CC</sub> = Min., I <sub>OH</sub> = -32 mA	2.0	3.0		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 64 mA		0.2	0.55	V

**Notes:**

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance.
- Operation beyond the limits set forth may impair the useful life of the device. Unless noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
- Typical values are at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = +25°C ambient.
- This parameter is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
- Tested at +25°C.

**Output Drive Characteristics for CY74FCT162240T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
I <sub>ODL</sub>	Output LOW Current <sup>[6]</sup>	V <sub>CC</sub> = 5V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> = 1.5V	60	115	150	mA
I <sub>ODH</sub>	Output HIGH Current <sup>[6]</sup>	V <sub>CC</sub> = 5V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> = 1.5V	-60	-115	-150	mA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -24 mA	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 24 mA		0.3	0.55	V

**Capacitance<sup>[5]</sup> (T<sub>A</sub> = +25°C, f = 1.0 MHz)**

Parameter	Description	Test Conditions	Typ. <sup>[4]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6.0	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8.0	pF

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[4]</sup>	Max.	Unit	
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> =Max. V <sub>IN</sub> ≤0.2V, V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	5	500	μA	
ΔI <sub>CC</sub>	Quiescent Power Supply Current (TTL inputs HIGH)	V <sub>CC</sub> =Max. V <sub>IN</sub> =3.4V <sup>[8]</sup>	0.5	1.5	mA	
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>[9]</sup>	V <sub>CC</sub> =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ =GND	60	100	μA/MHz	
I <sub>C</sub>	Total Power Supply Current <sup>[10]</sup>	V <sub>CC</sub> =Max., f <sub>1</sub> =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$ =GND	V <sub>IN</sub> =V <sub>CC</sub> or V <sub>IN</sub> =GND	0.6	1.5	mA
			V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	0.9	2.3	mA
		V <sub>CC</sub> =Max., f <sub>1</sub> =2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$ =GND	V <sub>IN</sub> =V <sub>CC</sub> or V <sub>IN</sub> =GND	2.4	4.5 <sup>[11]</sup>	mA
			V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	6.4	16.5 <sup>[11]</sup>	mA

**Notes:**

8. Per TTL driven input (V<sub>IN</sub>=3.4V); all other inputs at V<sub>CC</sub> or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 I<sub>CC</sub> = Quiescent Current with CMOS input levels  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL HIGH input (V<sub>IN</sub>=3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL inputs HIGH  
 N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current caused by an input transition pair (HLH or LHL)  
 f<sub>0</sub> = Clock frequency for registered devices, otherwise zero  
 f<sub>1</sub> = Input signal frequency  
 N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>  
 All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range<sup>[12]</sup>

Parameter	Description	CY74FCT16240AT		CY74FCT162240CT		Unit	Fig. No. <sup>[13]</sup>
		Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Output	1.5	4.8	1.5	4.3	ns	1, 2
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time	1.5	6.2	1.5	5.8	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	1.5	5.6	1.5	5.2	ns	1, 7, 8
t <sub>SK(O)</sub>	Output Skew <sup>[14]</sup>		0.5		0.5	ns	—

**Note:**

12. Minimum limits are specified but not tested on Propagation Delays.

13. See "Parameter Measurement Information" in the General Information section.

14. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

**Ordering Information CY74FCT16240**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.8	CY74FCT16240ATPVC/PVCT	O48	48-Lead (300-Mil) SSOP	Industrial

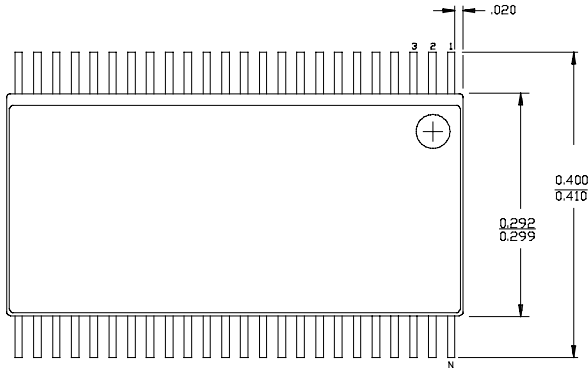
**Ordering Information CY74FCT162240**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	74FCT162240CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162240CTPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162240CTPVCT	O48	48-Lead (300-Mil) SSOP	

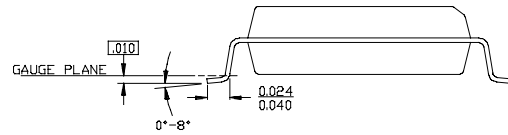
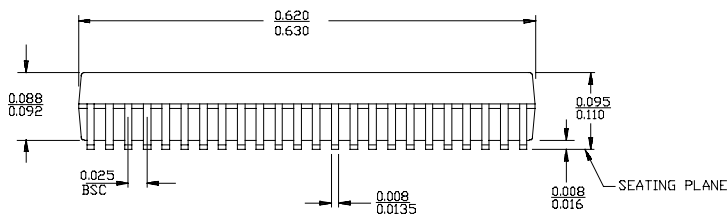
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**Package Diagrams**

**48-Lead Shrink Small Outline Package O48**

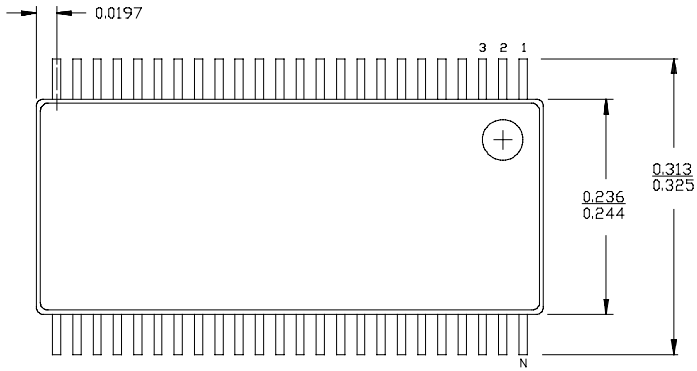


DIMENSIONS IN INCHES MIN.  
MAX.

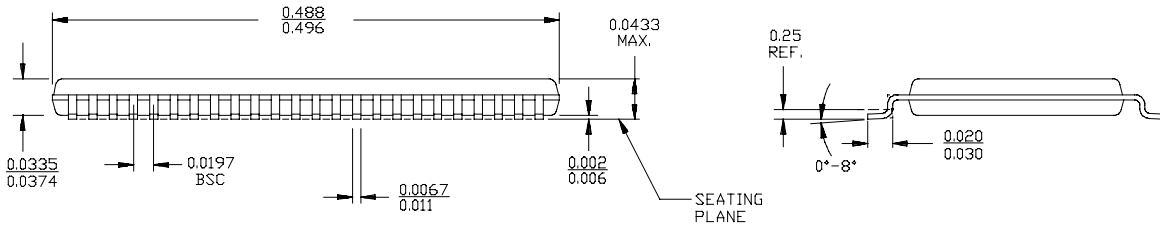


**Package Diagrams**

**48-Lead Thin Shrunken Small Outline Package**



DIMENSIONS IN INCHES MIN.  
MAX.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74FCT162240ATPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162240A	<a href="#">Samples</a>
74FCT162240CTPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162240C	<a href="#">Samples</a>
74FCT162240CTPVCG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162240C	<a href="#">Samples</a>
74FCT162240CTPVCT	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162240C	<a href="#">Samples</a>
74FCT162240ETPACT	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85		
74FCT162240ETPVCT	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI	-40 to 85		
74FCT16240ATPACTE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16240A	<a href="#">Samples</a>
74FCT16240ATPACTG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16240A	<a href="#">Samples</a>
74FCT16240ATPVCG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16240A	<a href="#">Samples</a>
74FCT16240ATPVCTG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16240A	<a href="#">Samples</a>
CY74FCT162240CTPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162240C	<a href="#">Samples</a>
CY74FCT162240ETPAC	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85		
CY74FCT162240ETPVC	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16240ATPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16240A	<a href="#">Samples</a>
CY74FCT16240ATPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16240A	<a href="#">Samples</a>
CY74FCT16240ATPVCT	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16240A	<a href="#">Samples</a>
CY74FCT16240ETPVC	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16240ETPVCT	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI	-40 to 85		
FCT162240ATPACTE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162240A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
FCT162240ATPACTG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162240A	<a href="#">Samples</a>
FCT162240CTPACTE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162240C	<a href="#">Samples</a>
FCT162240CTPACTG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162240C	<a href="#">Samples</a>
FCT162240CTPVCTG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162240C	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

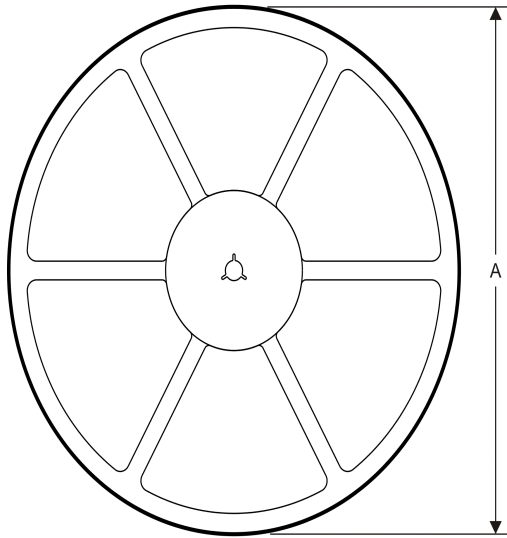
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**

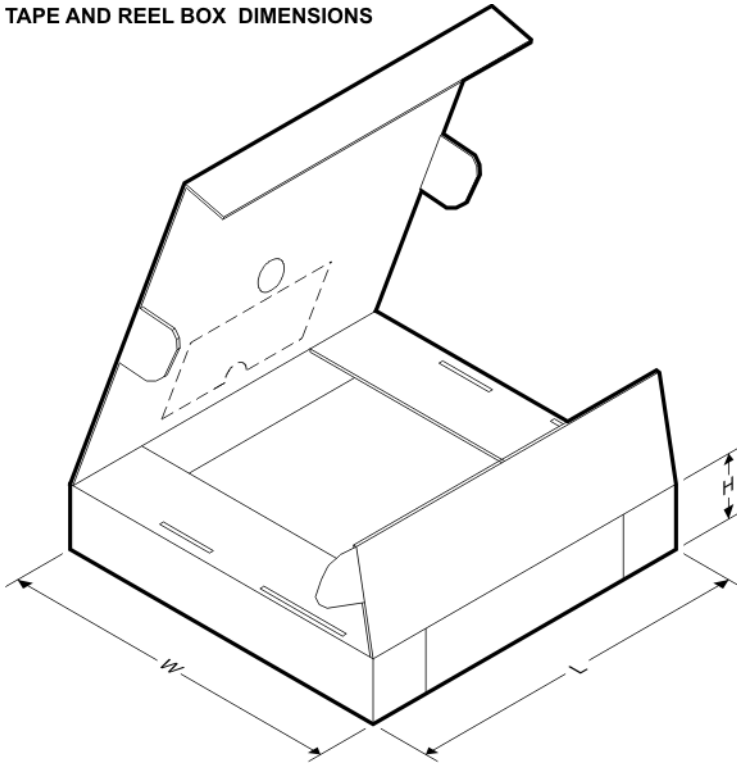

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74FCT162240ATPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
74FCT162240CTPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
74FCT162240CTPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
CY74FCT16240ATPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
CY74FCT16240ATPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

## TAPE AND REEL BOX DIMENSIONS



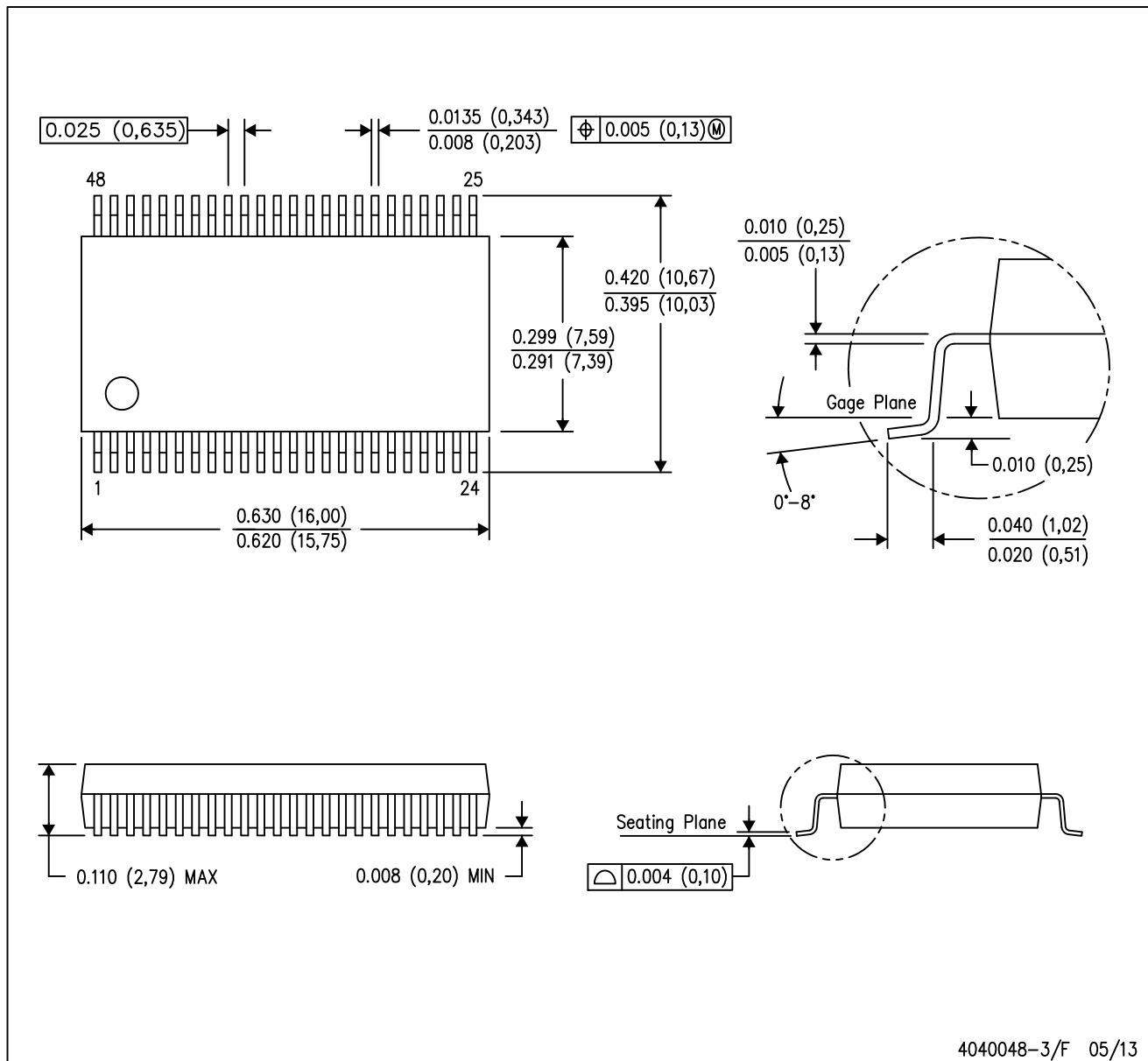
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74FCT162240ATPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0
74FCT162240CTPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0
74FCT162240CTPVCT	SSOP	DL	48	1000	367.0	367.0	55.0
CY74FCT16240ATPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0
CY74FCT16240ATPVCT	SSOP	DL	48	1000	367.0	367.0	55.0

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



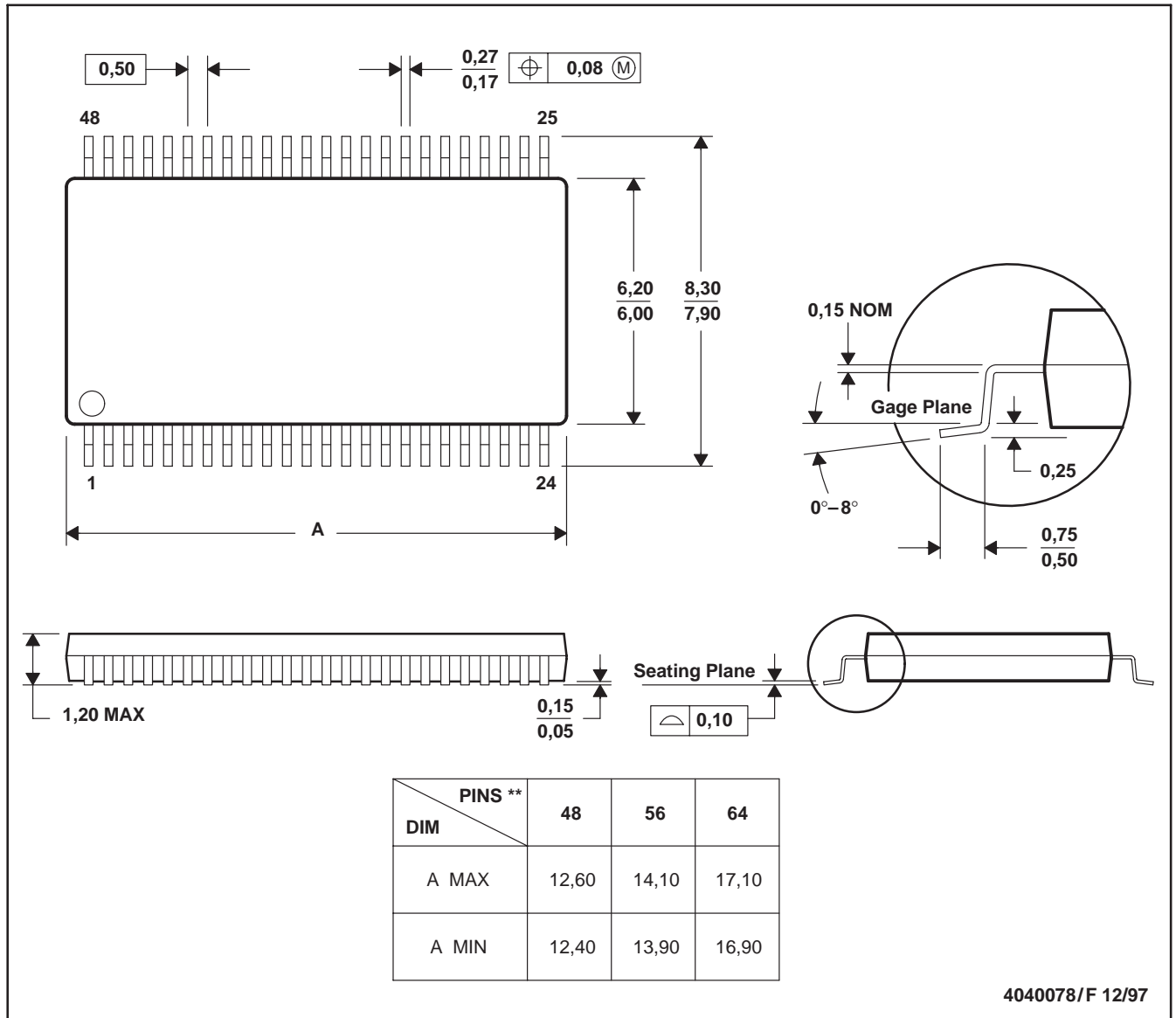
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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