



High Speed CMOS Bus Interface 8-Bit Latches

QS54/74FCT373T
QS54/74FCT533T*

QS54/74FCT2373T
QS54/74FCT2533T*

FEATURES/BENEFITS

- Pin and function compatible to the 74F373/533 74FCT373/533 and 74ABT373/533
- CMOS power levels: <7.5 mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 373T, 533T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std., A, C, and D speed grades with 3.7 ns for D
- $I_{OL} = 48$ mA Com., 32 mA Mil.

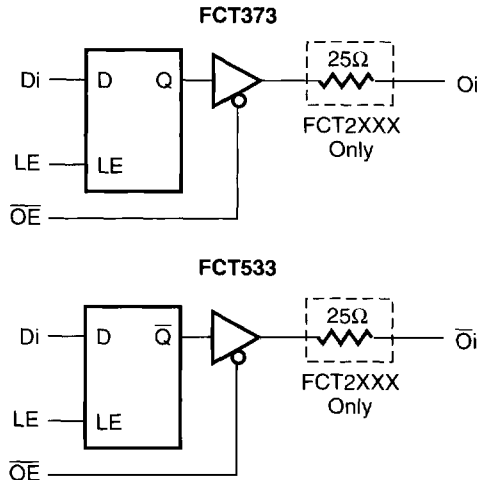
FCT-T 2373T, 2533T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A, C, and D speed grades with 3.7 ns for D
- $I_{OL} = 12$ mA Com.

DESCRIPTION

The QSFCT373T and QSFCT533T are 8-bit high-speed CMOS TTL-compatible buffered latches with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2373 and 2533 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2373 and 2533 series parts can replace 373 and 533 devices in existing designs to reduce noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

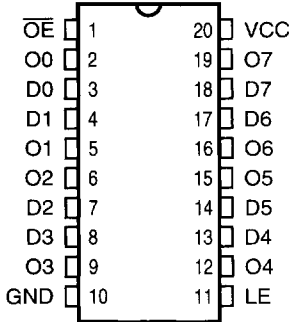
FUNCTIONAL BLOCK DIAGRAM



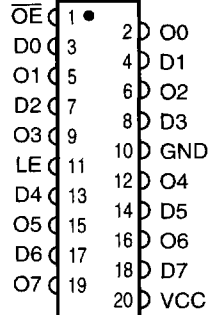
*Note: QS54/74FCT533T and QS54/74FCT2533T are not recommended for use in new designs

PIN CONFIGURATIONS (All Pins Top View)

PDIP, SOIC, QSOP, HQSOP



ZIP



PIN DESCRIPTION

Name	I/O	Description
Di	I	Data Inputs
O _i	O	Data Outputs
LE	I	Latch Enable
\overline{OE}	I	Output Enable

FUNCTION TABLE

\overline{OE}	Inputs		Internal Q Value	Outputs		Function
	LE	Di		373 O _i	533 $\overline{O_i}$	
H	X	X	X	Hi-Z	Hi-Z	Disable Outputs
L	L	X	H	H	L	Enable Outputs
L	L	X	L	L	H	
L	H	L	L	L	H	Pass Inputs
L	H	H	H	H	L	
L	L	X	Q	Q	\overline{Q}	Hold Prior Data

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	-0.5V to +7.0V
DC Output Voltage V_{OUT}	-0.5V to +7.0V
DC Input Voltage V_{IN}	-0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Input Diode Current with $V_{IN} < 0$	-20 mA
DC Output Diode Current with $V_{OUT} < 0$	-50 mA
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
TSTG Storage Temperature	-65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1$ MHz, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1, 3, 4, 7, 8, 11, 13, 14, 17, 18	4	4	5	7	pF
2, 5, 6, 9, 12, 15, 16, 19	6	6	7	9	pF
—	8	8	9	10	pF

Note: Capacitance is characterized but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Max	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC}-0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}$, $V_{IN} = 3.4\text{V}$, freq = 0 ⁽²⁾	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$, Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or V_{CC} ^(3,4)	—	0.25	mA/ MHz

Notes:

- For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
- Per TTL driven input ($V_{IN} = 3.4\text{V}$).
- For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
- I_C can be computed using the above parameters as explained in the Technical Overview section.

QSFCT373T, 533T, 2373T, 2533T

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 5\%$

Military $T_A = -55^\circ\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	μA
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$	—	—	5	μA
I_{OS}	Short Circuit Current (FCTXXX)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
I_{OR}	Current Drive (FCT2XXX - 25 Ω)	$V_{CC} = \text{Min.}, V_{OUT} = 2.0\text{V}^{(3)}$	50	—	—	mA
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}, T_A = 25^\circ\text{C}^{(3)}$	—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -12 \text{ mA (MIL)}$ $I_{OH} = -15 \text{ mA (COM)}$	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage (FCTXXX)	$V_{CC} = \text{Min.}$ $I_{OL} = 32 \text{ mA (MIL)}$ $I_{OL} = 48 \text{ mA (COM)}$	— —	— —	0.50 0.50	V
V_{OL}	Output LOW Voltage (FCT2XXX - 25 Ω)	$V_{CC} = \text{Min.}$ $I_{OL} = 12 \text{ mA (MIL)}$ $I_{OL} = 12 \text{ mA (COM)}$	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance (FCT2XXX - 25 Ω)	$V_{CC} = \text{Min.}$ $I_{OL} = 12 \text{ mA (MIL)}$ $I_{OL} = 12 \text{ mA (COM)}$	— 20	25 28	— 40	Ω

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Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, V_{cc} = 5.0V ± 5%

Military T_A = -55°C to 125°C, V_{cc} = 5.0V ± 10%

C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description ⁽¹⁾		373 533 2373 2533		373A 533A 2373A 2533A		373C 533C 2373C 2533C		373D 533D 2373D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PHL}	Propagation Delay	COM	1.5	8	1.5	5.2	1.5	4.2	1.5	3.7	ns
t _{PLH}	Data to O _i , 373	MIL	2	8.5	1.5	5.6	1.5	5.1	—	—	
t _{PHL}	Propagation Delay	COM	1.5	8	1.5	5.2	1.5	4.2	1.5	3.7	ns
t _{PLH}	Data to O _i , 2373	MIL	2	8.5	1.5	5.6	1.5	5.1	—	—	
t _{PHL}	Propagation Delay	COM	2	13	2	8.5	2	5.5	2	4.9	ns
t _{PLH}	LE to O _i , 373	MIL	2	14	2	9.8	2	8	—	—	
t _{PHL}	Propagation Delay	COM	2	13	2	8.5	2	5.5	2	4.9	ns
t _{PLH}	LE to O _i , 2373	MIL	2	14	2	9.8	2	8	—	—	
t _{PZH}	Output Enable Time	COM	1.5	11	1.5	6.5	1.5	5.5	1.5	5.5	ns
t _{PZL}	\overline{OE} to Y _i , 373	MIL	1.5	12.5	1.5	7.5	1.5	6.3	—	—	
t _{PZH}	Output Enable Time	COM	1.5	11	1.5	6.5	1.5	6.2	1.5	6.2	ns
t _{PZL}	\overline{OE} to Y _i , 2373	MIL	1.5	12.5	1.5	7.5	1.5	7.2	—	—	
t _{PHZ}	Output Disable Time	COM ⁽²⁾	1.5	7	1.5	5.5	1.5	5.0	1.5	5.0	ns
t _{PLZ}	\overline{OE} to Y _i	MIL ⁽²⁾	1.5	8.5	1.5	6.5	1.5	5.9	—	—	
t _s	Data Setup Time	COM	2	—	2	—	2	—	2	—	ns
		MIL	2	—	2	—	2	—	—	—	
t _H	Data Hold Time	COM	1.5	—	1.5	—	1.5	—	1.5	—	ns
		MIL	1.5	—	1.5	—	1.5	—	—	—	
t _w	LE Pulse Width	COM ⁽²⁾	6	—	5	—	4	—	4	—	ns
	HIGH or LOW	MIL ⁽²⁾	6	—	6	—	6	—	—	—	

Notes:

1. Minimums guaranteed but not tested for all parameters except t_s and t_H.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.