

P54/74FCT543/A (P54/74PCT543/A) P54/74FCT544/A (P54/74PCT544/A) OCTAL REGISTERED TRANSCEIVER

FEATURES

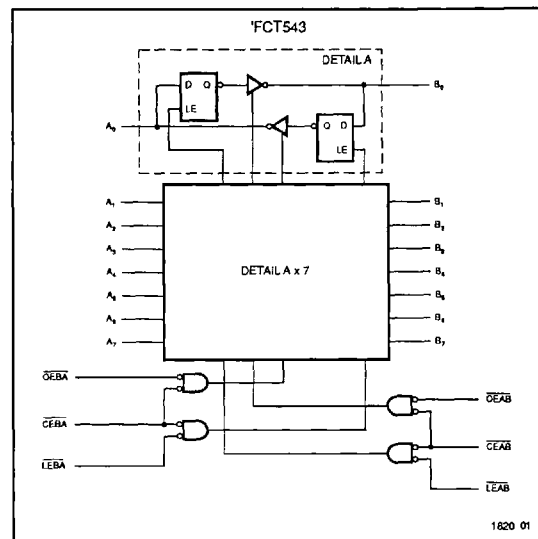
- Function, Pinout, and Drive Compatible with the FCT and F Logic
- FCT-A speed at 6.5ns max. (Com'I)
FCT speed at 8.5ns max. (Com'I)
- CMOS V_{OH} Levels for Low Power Consumption — Typically 1/3 of FAST Bipolar Logic
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Inputs and Outputs Interface Directly with TTL, NMOS, and CMOS Devices
- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode
- 64 mA Sink Current (Com'I), 48 mA (Mil)
15 mA Source Current (Com'I), 12 mA (Mil)
- Separate Controls for Data Flow in Each Direction
- Back to Back Latches for Storage
- 3-State Output
- Manufactured in 0.8 micron PACE Technology™

DESCRIPTION

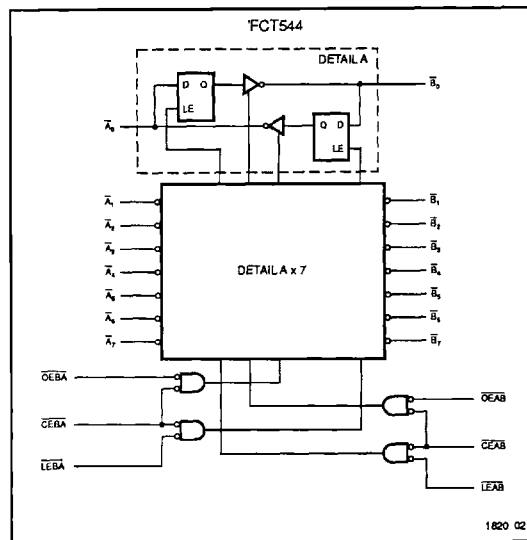
The 'FCT543 and 'FCT544 Octal Registered Transceivers contain two sets of eight D-type latches with separate Latch Enable (LEAB, LEBA) and Output Enable (OEAB, OEBA) controls for each set to permit independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B Enable (CEAB) input must be LOW in order to enter data from A0-A7 or to take data from B0-B7, as indicated in the truth table. With CEAB LOW, a LOW signal on the A-to-B Latch

Enable (LEAB) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the LEAB signal puts the A latches in the storage mode and their output no longer change with the A inputs. With CEAB and OEAB both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses CEAB, LEAB and OEAB inputs.

FUNCTIONAL BLOCK DIAGRAM

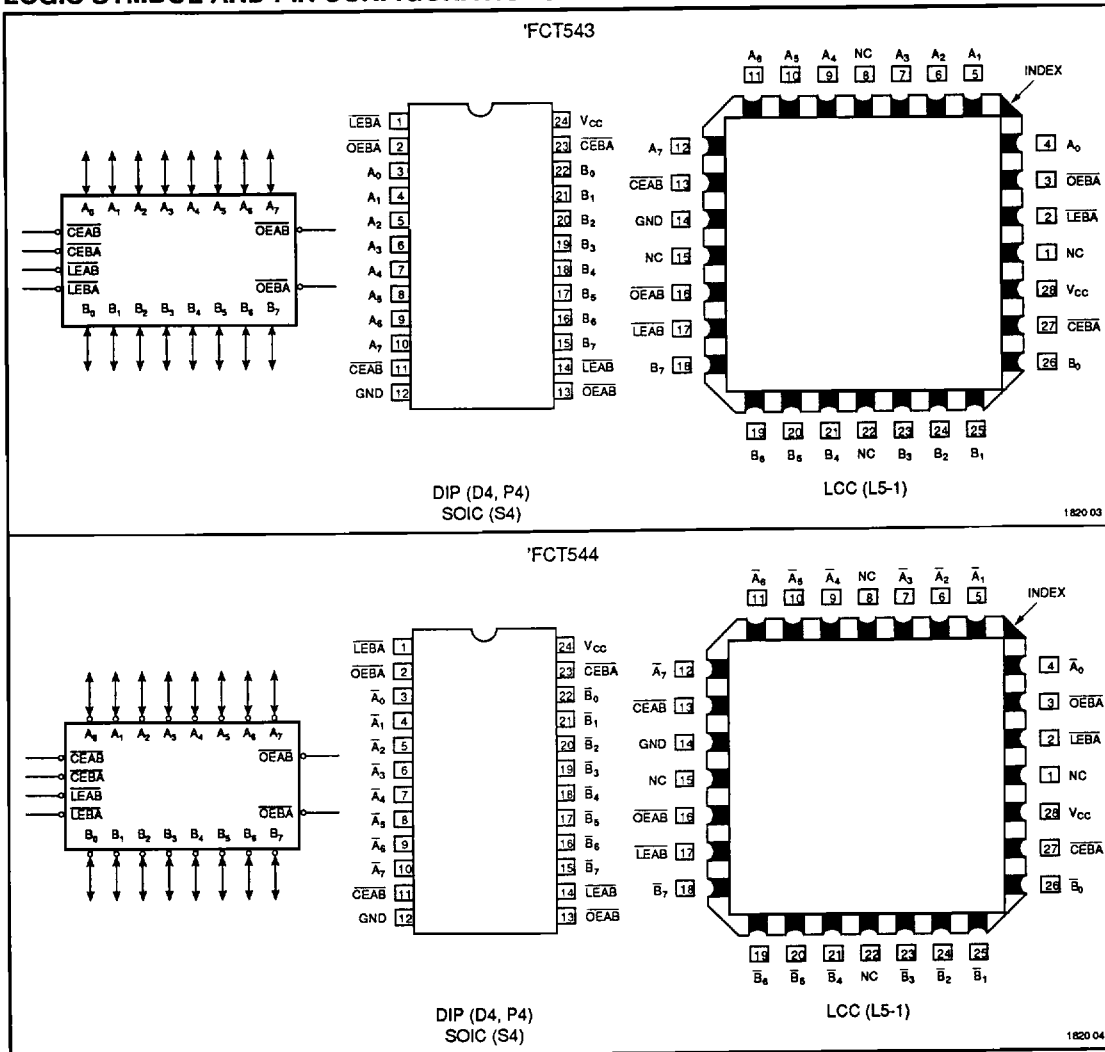


FUNCTIONAL BLOCK DIAGRAM



9

LOGIC SYMBOL AND PIN CONFIGURATIONS



PIN DESCRIPTIONS

| Pin Name | Description |
|-------------------|--|
| \overline{OEAB} | A-to-B Output Enable Input (Active LOW) |
| \overline{OEBA} | B-to-A Output Enable Input (Active LOW) |
| \overline{CEAB} | A-to-B Enable Input (Active LOW) |
| \overline{CEBA} | B-to-A Enable Input (Active LOW) |
| \overline{LEAB} | A-to-B Latch Enable Input (Active LOW) |
| \overline{LEBA} | B-to-A Latch Enable Input (Active LOW) |
| A_0 – A_7 | A-to-B Data Inputs or B-to-A 3-State Outputs |
| B_0 – B_7 | B-to-A Data Inputs or A-to-B 3-State Outputs |

ABSOLUTE MAXIMUM RATINGS^{1,2}

| Symbol | Parameter | Value | Unit |
|------------------|-------------------------------------|--------------|------|
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| T _A | Ambient Temperature Under Bias | -65 to +135 | °C |
| V _{CC} | V _{CC} Potential to Ground | -0.5 to +7.0 | V |
| I _{IN} | Input Current | -30 to +5.0 | mA |

Notes:

1820 TH 02

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

| Symbol | Parameter | Value | Unit |
|---------------------|---------------------------|-------------------------------|------|
| I _{OUTPUT} | Current Applied to Output | 120 | mA |
| V _{IN} | Input Voltage | -0.5 to V _{CC} + 0.5 | V |
| V _{OUT} | Voltage Applied to Output | -0.5 to V _{CC} + 0.5 | V |

1820 TH 03

2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

| Free Air Ambient Temperature | Min | Max |
|------------------------------|-------|--------|
| Military | -55°C | +125°C |
| Commercial | 0°C | +70°C |

1820 TH 04

| Supply Voltage (V _{CC}) | Min | Max |
|-----------------------------------|--------|--------|
| Military | +4.5V | +5.5V |
| Commercial | +4.75V | +5.25V |

1820 TH 05

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

| Symbol | Parameter | Min | Typ ¹ | Max | Units | V _{CC} | Conditions | |
|------------------|---|---|-----------------------|-----------------|-------|-----------------|-----------------------------------|-------------------------|
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | | |
| V _{IL} | Input LOW Voltage | | 0.8 | V | | | | |
| V _H | Hysteresis | | 0.35 | | V | | All inputs | |
| V _{CD} | Input Clamp Diode Voltage | | -0.7 | -1.2 | V | MIN | I _{IN} = -18mA | |
| V _{OH} | Output HIGH Voltage | V _{CC} = 3V, V _{IN} = 0.2V, or V _{CC} - 0.2V | V _{CC} - 0.2 | V _{CC} | V | | I _{OH} = -32µA | |
| | | Military/Commercial (CMOS) | V _{CC} - 0.2 | V _{CC} | V | MIN | I _{OH} = -300µA | |
| | | Military (TTL) | 2.4 | 4.3 | V | MIN | I _{OH} = -12mA | |
| | | Commercial (TTL) | 2.4 | 4.3 | V | MIN | I _{OH} = -15mA | |
| V _{OL} | Output LOW Voltage | V _{CC} = 3V, V _{IN} = 0.2V, or V _{CC} - 0.2V | | GND | 0.2 | V | I _{OL} = 300µA | |
| | | Military/Commercial (CMOS) | | GND | 0.2 | V | MIN | I _{OL} = 300µA |
| | | Military (TTL) | | 0.3 | 0.55 | V | MIN | I _{OL} = 48mA |
| | | Commercial (TTL) | | 0.3 | 0.55 | V | MIN | I _{OL} = 64mA |
| I _{IH} | Input HIGH Current (Except I/O Pins) | | | 5 | µA | MAX | V _{IN} = V _{CC} | |
| I _{IL} | Input LOW Current (Except I/O Pins) | | | -5 | µA | MAX | V _{IN} = GND | |
| I _{IH} | Input HIGH Current ³ (Except I/O Pins) | | | 5 | µA | MAX | V _{IN} = 2.7V | |
| I _{IL} | Input LOW Current ³ (Except I/O Pins) | | | -5 | µA | MAX | V _{IN} = 0.5V | |
| I _{IH} | Input HIGH Current (I/O Pins only) | | | 15 | µA | MAX | V _{IN} = V _{CC} | |
| I _{IL} | Input LOW Current (I/O Pins only) | | | -15 | µA | MAX | V _{IN} = GND | |
| I _{IH} | Input HIGH Current ³ (I/O Pins only) | | | 15 | µA | MAX | V _{IN} = 2.7V | |
| I _{IL} | Input LOW Current ³ (I/O Pins only) | | | -15 | µA | MAX | V _{IN} = 0.5V | |
| I _{OS} | Output Short Circuit Current ² | -60 | -120 | | mA | MAX | V _{OUT} = 0.0V | |
| C _{IN} | Input Capacitance ³ | | 5 | 10 | pF | | All inputs | |
| C _{OUT} | Output Capacitance ³ | | 9 | 12 | pF | | All outputs | |

Notes:

1820 TH 06

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
 2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

| Symbol | Parameter | Typ. ¹ | Max. | Units | Conditions |
|-----------------|--|-------------------|-------------------|------------|---|
| I_{CC} | Quiescent Power Supply Current (CMOS inputs) | 0.003 | 0.5 | mA | $V_{CC} = \text{MAX}$, $f_1 = 0$, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ |
| ΔI_{CC} | Quiescent Power Supply Current (TTL inputs) | 0.5 | 2.0 | mA | $V_{CC} = \text{MAX}$, $V_{IN} = 3.4V^2$, $f_1 = 0$, Outputs Open |
| I_{CCD} | Dynamic Power Supply Current ³ | 0.15 | 0.25 | mA/ mHz | $V_{CC} = \text{MAX}$, One Input Toggling, 50% Duty Cycle, $\overline{CEAB} + \overline{OEAB} = \text{Low}$, Outputs Open, $\overline{CEAB} = \text{High}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ |
| I_C | Total Power Supply Current ⁵ | 1.7 | 4.0 | mA | $V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, $\overline{CEAB} + \overline{OEAB} = \text{Low}$ 50% Duty Cycle, Outputs Open, $\overline{CEBA} = \text{High}$ One Bit Toggling at $f_1 = 5\text{MHz}$, $f_0 = \overline{LEAB} = 10\text{MHz}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ |
| | | 2.2 | 6.0 | mA | $V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, $\overline{CEAB} + \overline{OEAB} = \text{Low}$ 50% Duty Cycle, Outputs Open, $\overline{CEBA} = \text{High}$ One Bit Toggling at $f_1 = 5\text{MHz}$, $f_0 = \overline{LEAB} = 10\text{MHz}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$ |
| | | 7.0 | 12.8 ⁴ | mA | $V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, $\overline{CEAB} + \overline{OEAB} = \text{Low}$ 50% Duty Cycle, Outputs Open, $\overline{CEBA} = \text{High}$ Eight Bits Toggling at $f_1 = 5\text{MHz}$, $f_0 = \overline{LEAB} = 10\text{MHz}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ |
| | | 9.2 | 21.8 ⁴ | mA | $V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, $\overline{CEAB} + \overline{OEAB} = \text{Low}$ 50% Duty Cycle, Outputs Open, $\overline{CEBA} = \text{High}$ Eight Bits Toggling at $f_1 = 5\text{MHz}$, $f_0 = \overline{LEAB} = 10\text{MHz}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$ |

1820 Tbl 09

Notes:

- Typical values are at $V_{CC} = 5.0V$, +25°C ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_n N_T + I_{CCD} (f_0/2 + f_1 N_i)$
 $I_{CC} = \text{Quiescent Current with CMOS input levels}$

$\Delta I_{CC} =$ Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

$D_n =$ Duty Cycle for TTL Inputs High

$N_T =$ Number of TTL Inputs at D_n

$I_{CCD} =$ Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

$f_0 =$ Clock Frequency for Register Devices (Zero for Non-Register Devices)

$f_1 =$ Input Frequency

$N_i =$ Number of Inputs at f_1

All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE FOR A-TO-B (Symmetric with B-to-A)

| Inputs | | | Latch Status | Outputs 'FCT543 | Outputs 'FCT544 |
|--------|------|------|--------------|-------------------|-------------------|
| CEAB | LEAB | OEAB | A-TO-B | B0-B7 | B0-B7 |
| H | - | - | Storing | High Z | High Z |
| - | H | - | Storing | - | - |
| - | - | H | - | High Z | High Z |
| L | L | L | Transparent | Current A Inputs | Previous A Inputs |
| L | H | L | Storing | Previous A Inputs | Current A Inputs |

* = Before \overline{LEAB} LOW-to-HIGH Transition

H = HIGH Voltage Level

L = LOW Voltage Level

- = Don't Care or Irrelevant

A-to-B data flow shown: B-to-A flow control is the same, except using \overline{CEBA} , \overline{LEBA} , and \overline{OEBA}

1820 Tbl 10

AC CHARACTERISTICS

| Sym. | Parameter | 'FCT543 'FCT544 | | | | 'FCT543A 'FCT544A | | | | Units | Fig. No. |
|--------------------------------------|---|--------------------|------|-------------------|------|----------------------|------|-------------------|------|-------|----------|
| | | MIL | | COM'L | | MIL | | COM'L | | | |
| | | Min. ¹ | Max. | Min. ¹ | Max. | Min. ¹ | Max. | Min. ¹ | Max. | | |
| t _{PLH} t _{PHL} | Propagation Delay Transparent Mode A _n to B _n or B _n to A _n | 2.0 | 10.0 | 2.5 | 8.5 | 2.5 | 7.5 | 2.5 | 6.5 | ns | 1, 5 |
| t _{PLH} t _{PHL} | Propagation Delay LEBA to A _n LEAB to B _n | 2.5 | 14.0 | 2.5 | 12.5 | 2.5 | 9.0 | 2.5 | 8.0 | ns | 1, 5 |
| t _{PZH} t _{PZL} | Output Enable Time OEBA or OEAB to A _n or B _n CEBA or CEAB to A _n or B _n | 2.0 | 14.0 | 2.0 | 12.0 | 2.0 | 10.0 | 2.0 | 9.0 | ns | 1,7,8 |
| t _{PHZ} t _{PLZ} | Output Disable Time OEBA or OEAB to A _n or B _n CEBA or CEAB to A _n or B _n | 2.0 | 13.0 | 2.0 | 9.0 | 2.0 | 8.5 | 2.0 | 7.5 | ns | 1,7,8 |

1820 Tbl 11

Note: Minimum limits are guaranteed on Propagation Delays.

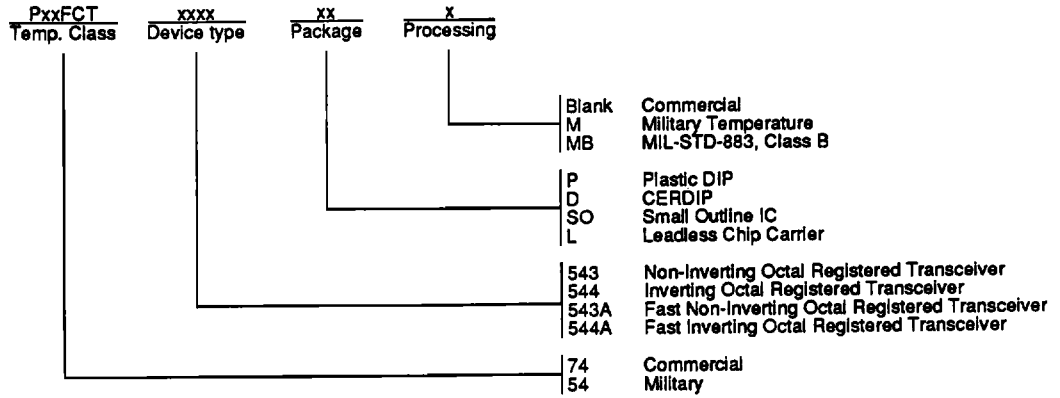
AC OPERATING REQUIREMENTS

| Sym. | Parameter | 'FCT543 'FCT544 | | | | 'FCT543A 'FCT544A | | | | Units | Fig. No. |
|--|---|--------------------|------|-------------------|------|----------------------|------|-------------------|------|-------|----------|
| | | MIL | | COM'L | | MIL | | COM'L | | | |
| | | Min. ¹ | Max. | Min. ¹ | Max. | Min. ¹ | Max. | Min. ¹ | Max. | | |
| t _s (H) t _s (L) | Set-up Time HIGH or LOW A _n or B _n to LEBA or LEAB | 3.0 | — | 3.0 | — | 2.0 | — | 2.0 | — | ns | 9 |
| t _h (H) t _h (L) | Hold Time HIGH or LOW A _n or B _n to LEBA or LEAB | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | ns | 9 |
| t _w | LEBA or LEAB Pulse Width LOW | 5.0 | — | 5.0 | — | 5.0 | — | 5.0 | — | ns | 6 |

1820 Tbl 12

9

ORDERING INFORMATION



1820 05