## CD54HC258/3A CD54HCT258/3A

#### **Burn-In Test-Circuit Connections**

Static		STATIC BURN-II	N I	STATIC BURN-IN II				
	OPEN	GROUND	V <sub>cc</sub> (6V)	OPEN	GROUND	V <sub>cc</sub> (6V)		
CD54HC/HCT258	4,7,9,12	1-3,5,6,8,10,11, 13-15	16	4,7,9,12	8	1-3,5,6,10,11,13-16		
			4 (0.14 (0.15		OSCILLATOR			
Dynamic	OPEN	GROUND	1/2 V <sub>cc</sub> (3V)	V <sub>cc</sub> (6V)	50 kHz	25 kHz		
CD54HC/HCT258	_	8,15	4,7,9,12	16	2,3,5,6,10,11, 13,14	1		

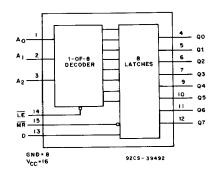
NOTE: Each pin except Vcc and Gnd will have a resistor of 2k-47k ohms.

## 8-Bit Addressable Latch

## CD54HC259/3A CD54HCT259/3A

The RCA-CD54HC259 and CD54HCT259 Addressable Latch features the low-power consumption associated with CMOS circuitry and has speeds comparable to low-power Schottky.

This latch has three active  $\underline{mode}$ s and one reset  $\underline{mode}$ . When both the Latch Enable (LE) and Master Reset ( $\overline{MR}$ ) inputs are low (8-line Demultiplexer mode) the output of the addressed latch follows the Data input and all other outputs are forced low. When both  $\overline{MR}$  and  $\overline{LE}$  are high (Memory latches hold the last data presented before the  $\overline{LE}$  transition from low to high. A condition of  $\overline{LE}$  low and  $\overline{MR}$  high (addressable Latch mode) allows the addressed latch's output to follow the data input; all other latches are unaffected. The Reset mode (all outputs low) results when  $\overline{LE}$  is high and  $\overline{MR}$  is low.



## **Package Specifications**

See Section 11, Fig. 11

### FUNCTIONAL DIAGRAM

#### Static Electrical Characteristics (Limits with black dots (•) are tested 100%)

				TEST	CONDITIO	NS				
						٧	IN			
			HC	/HCT		HC	HCT	LIMITS		
CHARACTERISTICS		V <sub>oD</sub> V <sub>o</sub> I <sub>o</sub>		V <sub>cc</sub> or GND	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>IL</sub> or V <sub>IH</sub>	MIN.	MAX.	UNITS	
Quiescent	25°C	6			6, 0			<u> </u>	8•	
Device Current	-55° C	6			6, 0	_	_	_	160•	μΑ
Icc	+125°C			]		<u> </u>		<u> </u>	<u> </u>	<u> </u>

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

## CD54HC259/3A CD54HCT259/3A

#### **HCT INPUT LOADING TABLE**

INPUT	UNIT LOAD*
A0-A2, LE	1.5
D	1.2
MR	0.75

<sup>\*</sup>Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

# Switching Speed (Limits with black dots (\*) are tested 100%.) SWITCHING CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> t<sub>r</sub> = 6 ns)

		TEST	LIMITS								
		CONDITIONS V <sub>cc</sub> V	25° C				-	-55°C to +125°C			
CHARACTERISTIC	SYMBOL		HC		HCT		54HC		54HCT		UNITS
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	]
Propagation Delay		2		185	_	_	_	280	-	_	
D to Q	İ	4.5	_	37∙	_	39•	—	56•	l —	59•	
		6		31	_	l —	_	48	—	_	
		2	_	170	_	I —	_	255	_	_	1
LE to Q		4.5	-	34•	_	38•	_	51∙	—	57•	
	t <sub>PLH</sub>	6	_	29	l —	l —	<u> </u>	43		1 —	
	t <sub>PHL</sub>	2	_	185	_	_	Г —	280		_	]
A to Q		4.5	l —	37•	l —	41•	<u> </u>	56•		61•	61• ns
		6		31	_	_	_	48	l —	_	
	7	2	_	155	-			235	_	l –	1
MR to Q		4.5		31•	—	39•	-	47•	—	59•	1
		6	<b> </b>	26		l —	_	40	—	l —	1
Output Transition		2	_	75	_	_	_	110	<u> </u>		1
Time	t <sub>TLH</sub>	4.5	—	15	l —	15	_	22	_	22	
	t <sub>THL</sub>	6		13	_	_		19	_	—	
Input Capacitance	Cı	_		10	_	10		10	_	10	pF

## Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static		STATIC BURN-	IN F	STATIC BURN-IN II			
	OPEN	GROUND	V <sub>cc</sub> (6V)	OPEN	GROUND	V <sub>cc</sub> (6V)	
CD54HC/HCT259	4-7,9-12	1-3,8,13-15	16	4-7,9-12	8	1-3,13-16	
D	OPEN	GROUND	1/2 V <sub>cc</sub> (3V)	V (6)()	OSCILLATOR		
Dynamic	OPEN	GROUND	1/2 Vcc (3V)	V <sub>cc</sub> (6V)	50 kHz	25 kHz	
CD54HC/HCT259		2,3,8,14	4-7,9-12	16	13,15	1	

NOTE: Each pin except Vcc and Gnd will have a resistor of 2k-47k ohms.