010223

Am93L21

Low-Power Dual Demultiplexer/One-of-Four Decoder

Distinctive Characteristics

- 45 mW typical power dissipation.
- Can act as dual four way demultiplexer.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Fan-out of three standard TTL circuits.

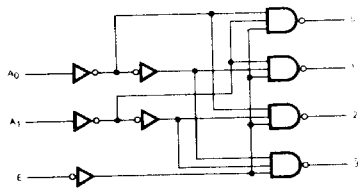
FUNCTIONAL DESCRIPTION

The Am93L21 low-power dual demultiplexer/one-of-four decoder consists of two identical independent decoders. Each decoder accepts two address inputs which select one-of-four mutually exclusive outputs. An active LOW enable is also provided on each decoder for expansion and demultiplexing applications. When this enable is at a HIGH logic level all the decoder outputs are forced HIGH.

In the demultiplexing mode data is presented at the enable input and appears noninverted at the selected output.

The Am93L21 is an ideal MSI element for use in decoding in high-speed memory systems.

LOGIC DIAGRAM



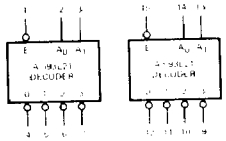
Note: Only one decoder shown.

LOADING RULES
In Units Loads (Notes)

Input Loading	TTL Loads HIGH	TTL Loads LOW	93L Loads HIGH	93L Loads LOW
All Inputs	0.5	0.25	1.0	1.0
Output Drive	**HIGH**	**LOW**	**HIGH**	**LOW**
All Outputs	10	3	12	12

Notes:
1. A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2. A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3. Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

Am93L21 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	93L21PC
Hermetic DIP	0°C to +75°C	93L21DC
Dice	0°C to +75°C	93L21XC
Hermetic DIP	−55°C to +125°C	93L21DM
Hermetic Flat Pak	−55°C to +125°C	93L21FM
Dice	−55°C to +125°C	93L21XM

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L21XC T_A = 0°C to +75°C V_{CC} = 4.75V to 5.25V
Am93L21XM T_A = −55°C to +125°C V_{CC} = 4.50V to 5.50V

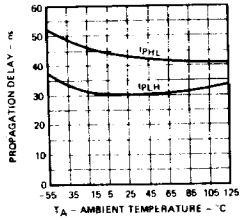
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	U
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.4mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		V
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92mA V_{IN} = V_{IH} or V_{IL}		0.15	0.3	V
V_{IH}	Input HIGH Level	Guaranteed input logic HIGH voltage for all inputs	2.0			V
V_{IL}	Input LOW Level	Guaranteed input logic LOW voltage for all inputs			0.7	V
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3V		−0.25	−0.4	
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V		2.0	20	
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V	−2.5	−16	−25	
I_{CC}	Power Supply Current	V_{CC} = MAX.		9.0	13.2	

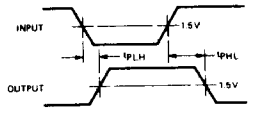
Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

Switching Characteristics (T_A = 25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	U
t_{PHL}	Delay Address to Output HIGH	V_{CC} = 5.0V C_L = 15pF		30	50	
t_{PLH}	Delay Address to Output LOW			43	65	
t_{PHL}	Delay Enable to Output HIGH			23	40	
t_{PLH}	Delay Enable to Output LOW			34	52	

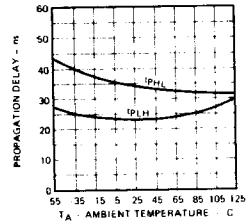
Address Input to Output

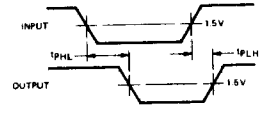




Other Conditions: Pins 15, 14 = GND

Enable Input to Output





Other Conditions: Pins 2, 3 = GND

ADVANC
MIC
DEVICES I
901 Thompson P
Sunny
California 9
(408) 732-
TWX: 910-339-
TELEX: 34-6

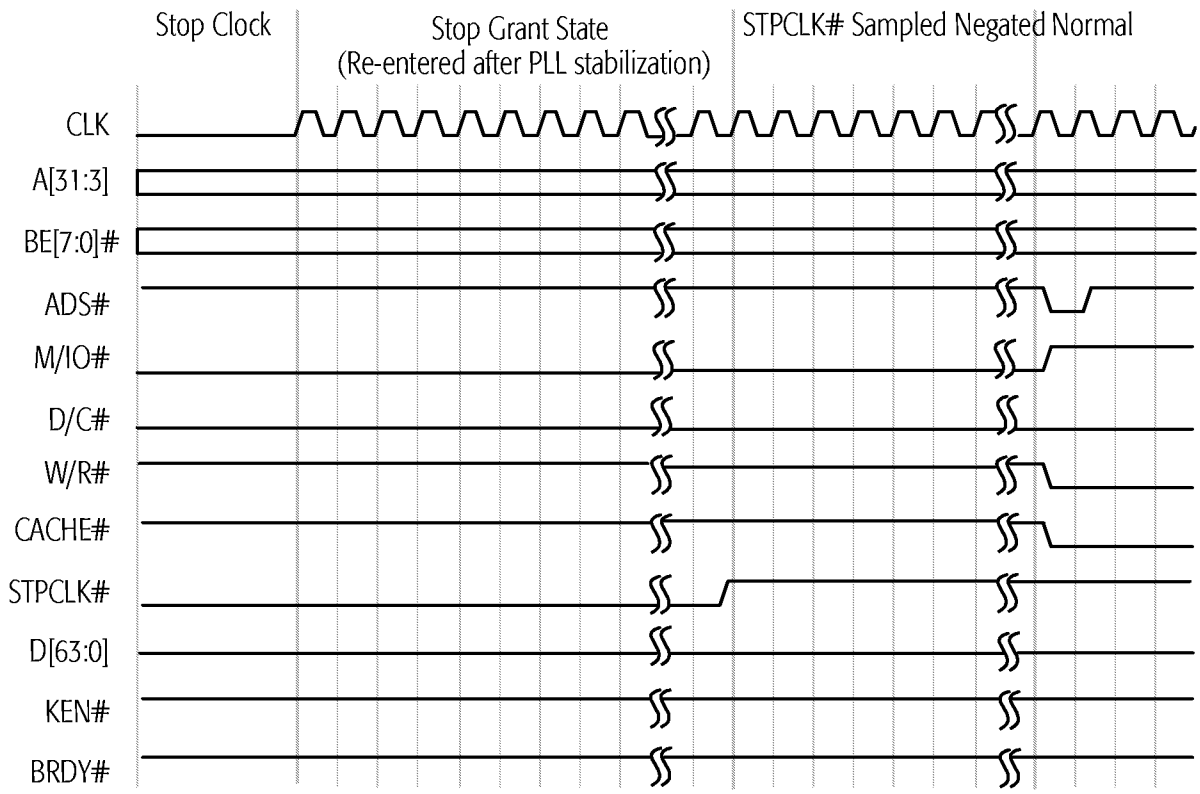


Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

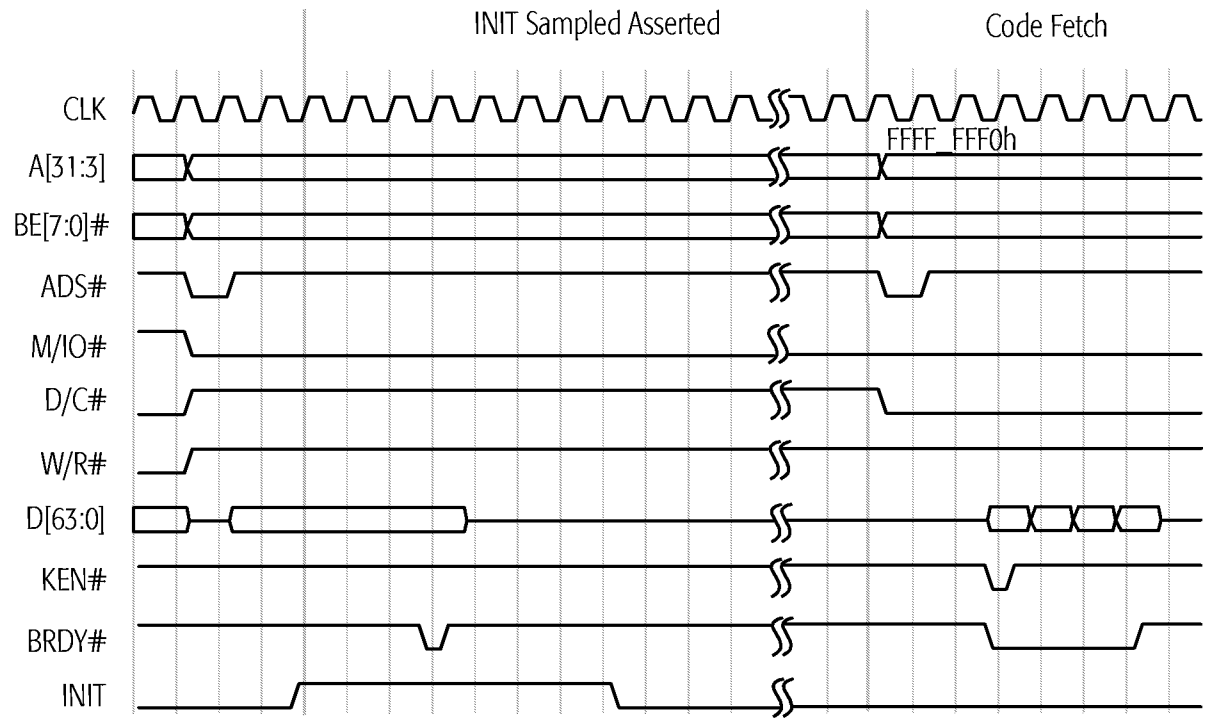


Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.