



# FAST CMOS OCTAL TRANSCEIVER/ REGISTERS (3-STATE)

**IDT74FCT2652T/AT/CT**

## FEATURES:

- Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
- Extended commercial range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$
- CMOS power levels
- True TTL input and output compatibility
  - $V_{OH} = 3.3\text{V}$  (typ.)
  - $V_{OL} = 0.3\text{V}$  (typ.)
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Available in PDIP, SOIC, SSOP, and QSOP packages
- Std., A, and C speed grades
- Resistor outputs (-15mA IOH, 12mA IOL)
- Reduced system switching noise

## DESCRIPTION:

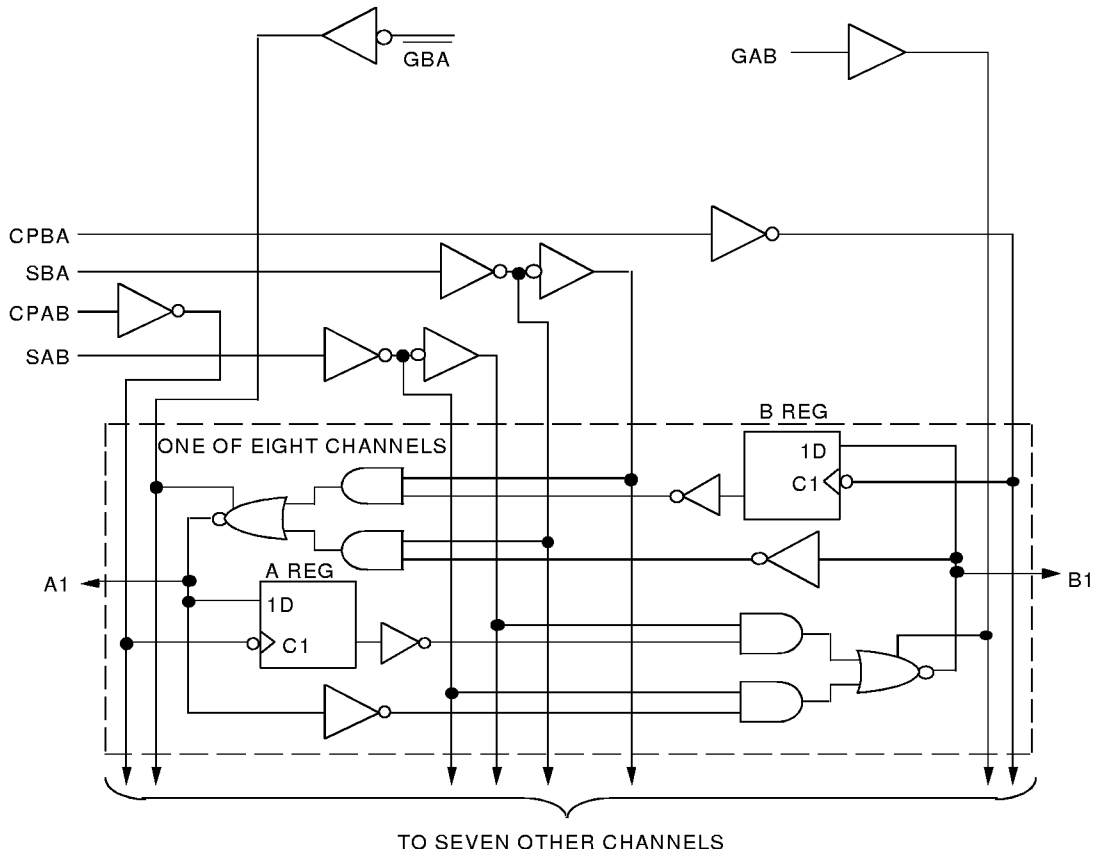
The FCT2652T consists of a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The FCT2652T utilizes GAB and  $\overline{\text{GBA}}$  signals to control the transceiver functions.

SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins.

The FCT2652T have balanced drive outputs with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. FCT2652T parts are plug-in replacements for FCT652T parts.

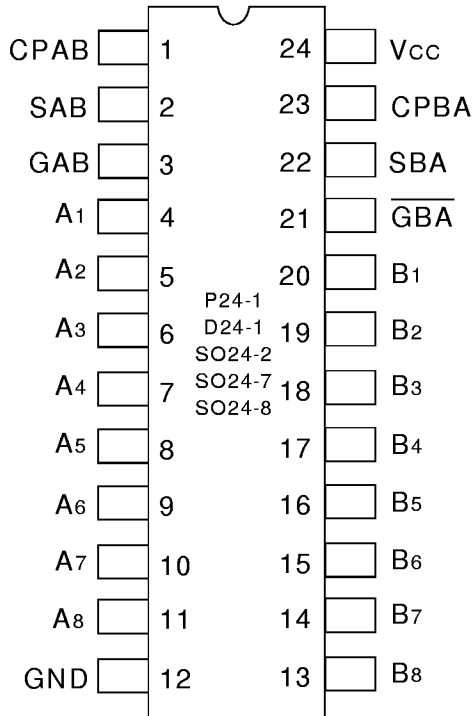
## FUNCTIONAL BLOCK DIAGRAM



**COMMERCIAL TEMPERATURE RANGE**

**SEPTEMBER 1999**

## PIN CONFIGURATION



PDIP/ SOIC/ SSOP/ QSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-65 to +120	mA

8T-link

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
- Inputs and V<sub>CC</sub> terminals only.
- Outputs and I/O terminals only.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

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### NOTE:

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Names	Description
A <sub>1</sub> - A <sub>8</sub>	Data Register A Inputs Data Register B Outputs
B <sub>1</sub> - B <sub>8</sub>	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
GAB, $\overline{\text{GBA}}$	Output Enable Inputs

## FUNCTION TABLE(2)

Inputs						Data I/O		Operation or Function
GAB	$\overline{\text{GBA}}$	CPAB	CPBA	SAB	SBA	A <sub>1</sub> - A <sub>8</sub>	B <sub>1</sub> - B <sub>8</sub>	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified <sup>(1)</sup>	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified <sup>(1)</sup>	Input	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

### NOTES:

1. The data output functions may be enabled or disabled by various signals at the GAB or  $\overline{\text{GBA}}$  inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

2. H = HIGH

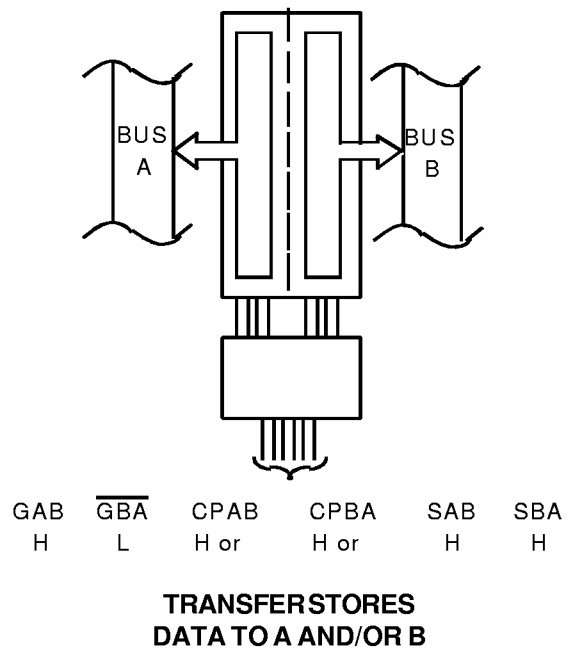
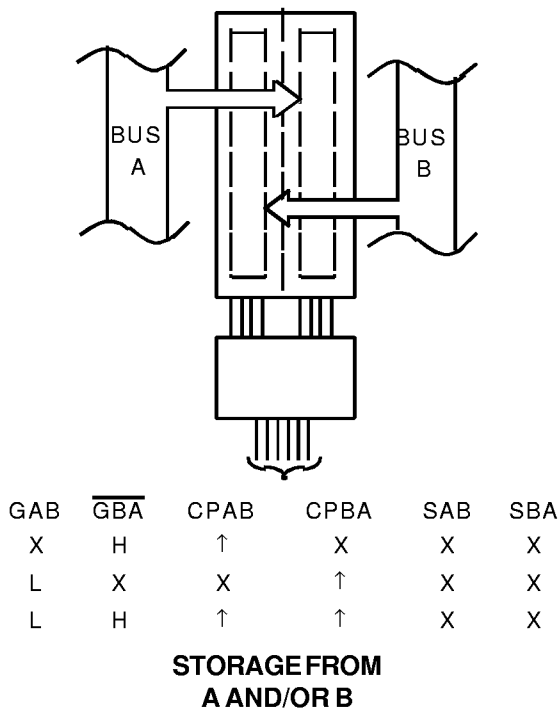
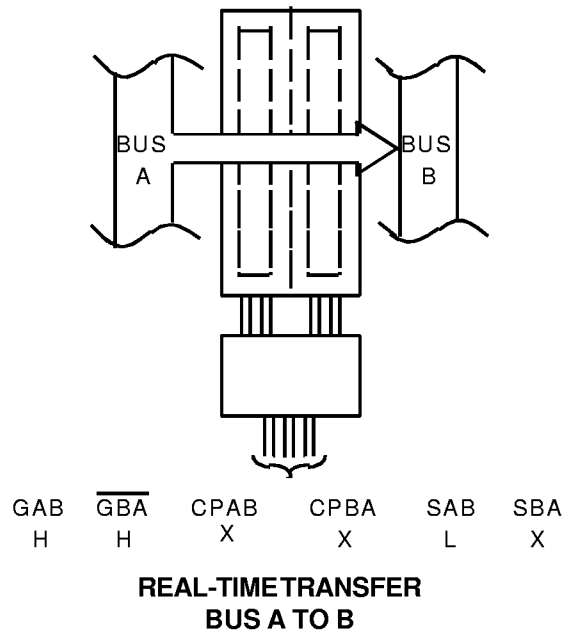
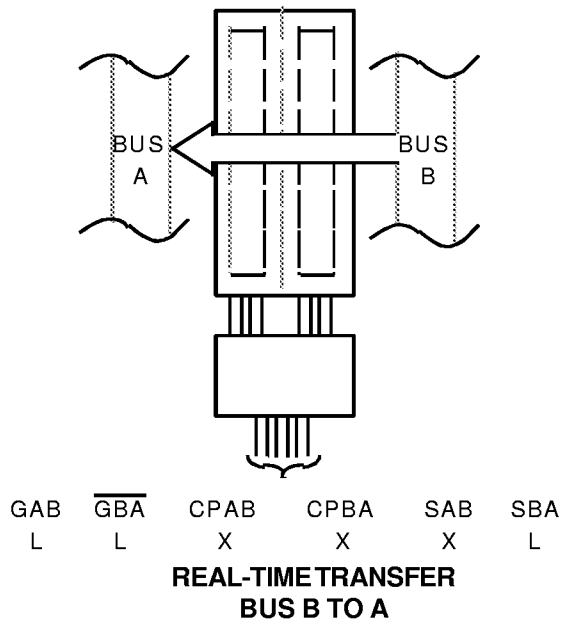
L = LOW

X = Don't Care

↑ = LOW-to-HIGH transition.

Select control = L: clocks can occur simultaneously.

Select control = H: clocks must be staggered in order to load both registers.



## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level	2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
$I_{IH}$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ $V_I = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{IL}$	Input LOW Current <sup>(4)</sup>		$V_I = 0.5\text{V}$	—	—	
$I_{OZH}$	High Impedance Output Current (3-State Output pins) <sup>(4)</sup>	$V_{CC} = \text{Max.}$ $V_O = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_O = 0.5\text{V}$	—	—	
$I_I$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$	—	—	$\pm 1$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
$V_H$	Input Hysteresis	—	—	200	—	mV
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$	—	0.01	1	mA

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_{ODL}$	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$	16	48	—	mA
$I_{ODH}$	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$	-16	-48	—	$\mu\text{A}$
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	2.4	3.3	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	—	0.3	0.5	V

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^\circ\text{C}$  ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^\circ\text{C}$ .
- This parameter is guaranteed but not tested.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>		—	0.5	2	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open G <sub>A</sub> B = $\overline{G}$ <sub>B</sub> A = GND One Input Toggling 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	0.06	0.12	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max. Outputs Open f <sub>CP</sub> = 10MHz 50% Duty Cycle G <sub>A</sub> B = $\overline{G}$ <sub>B</sub> A = GND One Bit Toggling at f <sub>i</sub> = 5MHz 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	0.6	2.2	mA
			V <sub>IN</sub> = 3.4 V <sub>IN</sub> = GND	—	1.1	4.2	
		V <sub>CC</sub> = Max. Outputs Open f <sub>CP</sub> = 10MHz 50% Duty Cycle G <sub>A</sub> B = $\overline{G}$ <sub>B</sub> A = GND Eight Bits Toggling at f <sub>i</sub> = 2.5MHz 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	1.5	4 <sup>(5)</sup>	
			V <sub>IN</sub> = 3.4 V <sub>IN</sub> = GND	—	3.8	13 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V). All other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 I<sub>CC</sub> = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>i</sub> = Input Frequency  
 N<sub>i</sub> = Number of Inputs at f<sub>i</sub>  
 All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

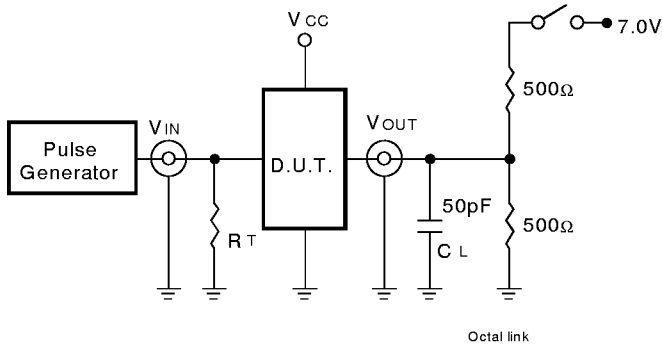
Symbol	Parameter	Condition <sup>(1)</sup>	FCT2652T		FCT2652AT		FCT2652CT		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Bus to Bus	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	2	9	2	6.3	1.5	5.4	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time, GAB, G <sub>B</sub> A to Bus		2	14	2	9.8	1.5	7.8	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time, GAB, G <sub>B</sub> A to Bus		2	9	2	6.3	1.5	6.3	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Bus		2	9	2	6.3	1.5	5.7	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay SBA or SAB to Bus		2	11	2	7.7	1.5	6.2	ns
t <sub>SU</sub>	Set-up Time HIGH or LOW Bus to Clock		4	—	2	—	2	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW Bus to Clock		2	—	1.5	—	1.5	—	ns
t <sub>w</sub>	Clock Pulse Width, HIGH or LOW <sup>(3)</sup>		6	—	5	—	5	—	ns

### NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

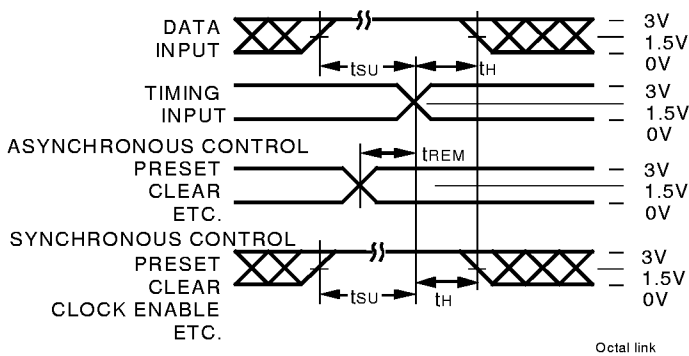
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#### DEFINITIONS:

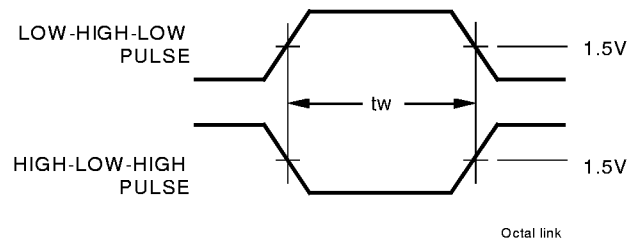
$C_L$  = Load capacitance: includes jig and probe capacitance.

$R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

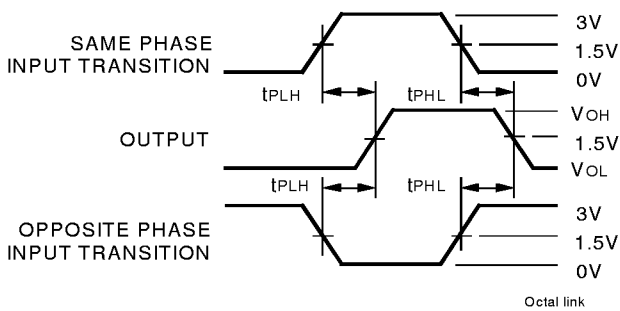
### SET-UP, HOLD, AND RELEASE TIMES



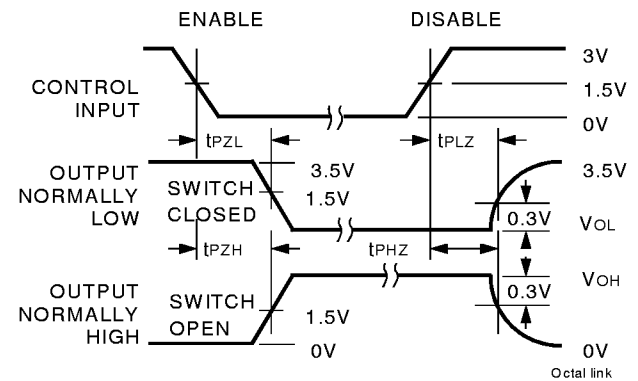
### PULSE WIDTH



### PROPAGATION DELAY



### ENABLE AND DISABLE TIMES

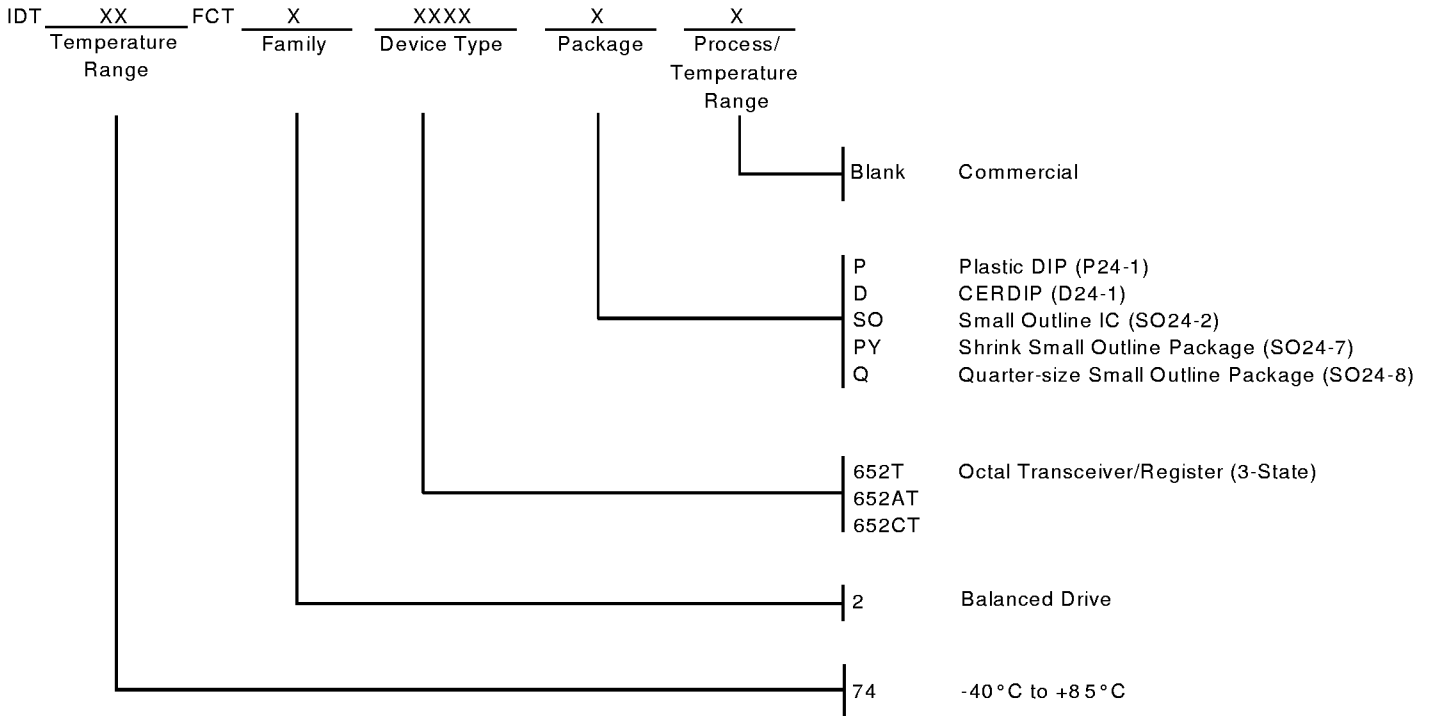


#### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_F \leq 2.5\text{ns}$ ;  $t_R \leq 2.5\text{ns}$



**ORDERING INFORMATION**



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