MOTOROLA

Military 10541

Four Bit Universal Shift Register

ELECTRICALLY TESTED PER:
5962-8855701

The 10541 is a four-bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Input S_1 and S_2 control the four possible operations of the register without external gating of the clock.

The flip-flops shift information on the positive edge of the dock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

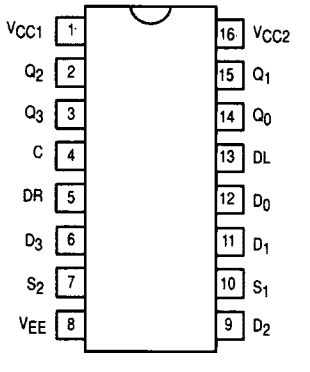
- 585 mW Max/Pkg (No Load)
- f_{Shift} = 200 MHz typ
- t_r, t_f = 1.5 ns typ (20% - 80%)

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8855701
3) 883: 10541/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

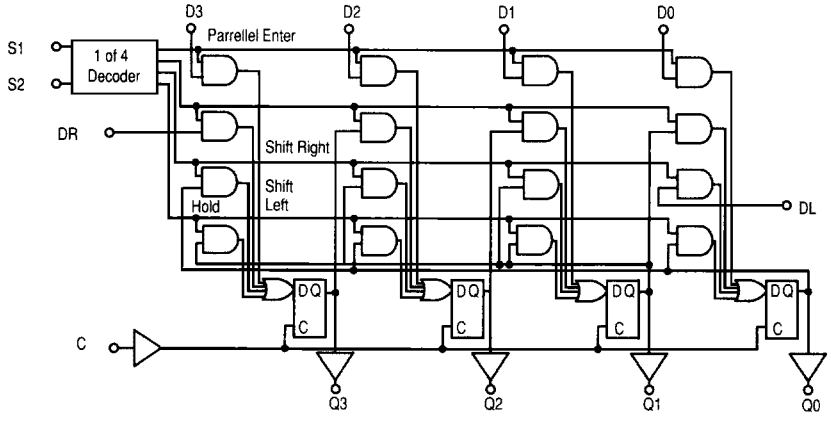


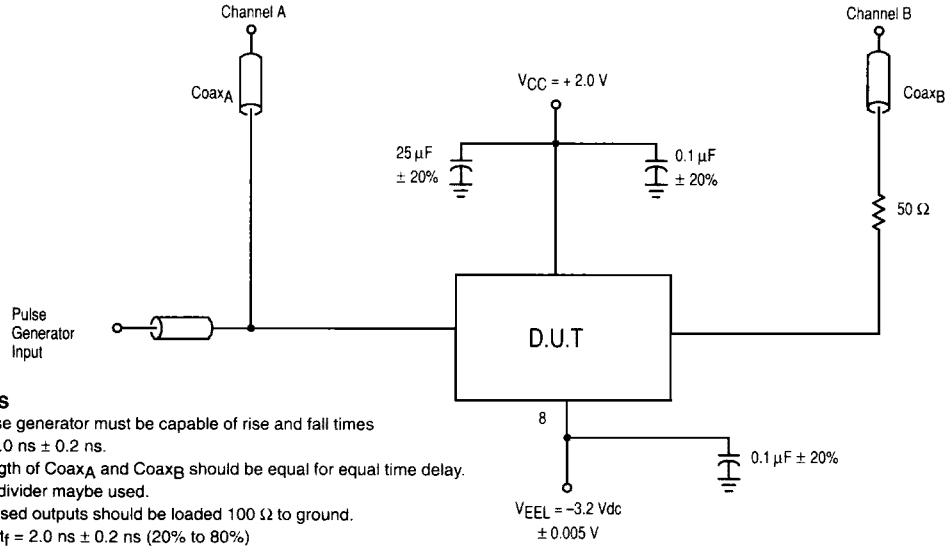
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_2	2	6	3	51 Ω to V_{TT}
Q_3	3	7	4	51 Ω to V_{TT}
C	4	8	5	CP1
DR	5	9	7	OPEN
D_3	6	10	8	GND
S_2	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
D_2	9	13	12	GND
S_1	10	14	13	OPEN
D_1	11	15	14	GND
D_0	12	16	15	GND
DL	13	1	17	OPEN
Q_0	14	2	18	51 Ω to V_{TT}
Q_1	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

LOGIC DIAGRAM





NOTES

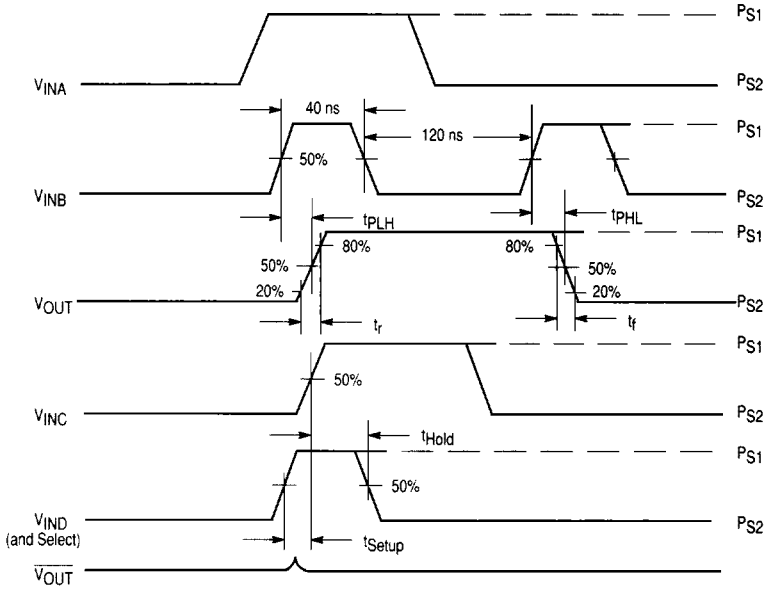
1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
3. 3:1 divider maybe used.
4. Unused outputs should be loaded 100 Ω to ground.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%)

Figure 1. Switching Test Circuit and Waveforms

TRUTH TABLE

SELECT		OPERATING MODE	OUTPUTS			
S_1	S_2		Q_{0n+1}	Q_{1n+1}	Q_{2n+1}	Q_{3n+1}
L	L	Parallel Entry	D_0	D_1	D_2	D_3
L	H	Shift Right *	$Q1_n$	Q2n	Q3n	DR
H	L	Shift Left *	DL	Q0n	Q1n	Q2n
H	H	Stop Shift	$Q0_n$	Q1n	Q2n	Q3n

* Outputs as exist after pulse at "C" input conditions as shown,
(Pulse = Positive transition of the clock input.).



NOTES

1. V_{IN} has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 2.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.

Figure 2. Switching Test Circuit Waveforms

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QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	4, 5, 9, 11, 12	4			8	1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	4	4, 5, 9, 11, 12			8	1, 16	2, 3, 14, 15
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	4 - 7, 9 - 13	4 - 7, 9 - 13	4 - 7, 9 - 13	4 - 7, 9 - 13	8	1, 16	2 - 4, 13 - 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	4 - 7, 9 - 13	4 - 7, 9 - 13	4 - 7, 9 - 13	4 - 7, 9 - 13	8	1, 16	2 - 4, 13 - 15
I_{IH1}	Input Current High		220		375		375	µA	5, 6, 9, 11 - 13				8	1, 16	5, 6, 9, 11 - 13
I_{IH2}	Input Current High		245		415		415	µA	7, 10				8	1, 16	7, 10
I_{IH3}	Input Current High		265		450		450	µA	4				8	1, 16	4
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 13			8	1, 16	4 - 7, 9 - 13
I_{EE}	Power Supply Drain Current	- 102		- 112		- 112		mA					8	1, 16	8

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		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.0	3.9	1.0	3.6	ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time	1.1	3.3	1.0	3.9	1.0	3.6	ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PHL}	Propagation Delay	1.8	3.8	2.0	4.5	1.7	4.1	ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH}	Propagation Delay	1.8	3.8	2.0	4.5	1.7	4.1	ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{Setup}	Setup Time Data Input	2.5		3.0		3.0		ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{hold}	Hold Time Data Input	1.5		1.5		1.5		ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{Setup}	Setup Time Select Inputs	5.0		7.0		7.0		ns	4, 6, 9, 11, 12	3, 14	1, 16	8	2, 3, 14, 15
t_{hold}	Hold Time Select Input	1.5		1.5		1.5		ns	4, 6, 9, 11, 12	3, 14	1, 16	8	2, 3, 14, 15
f_{tog}	Toggle Frequency	150		150		150		MHz	4, 6, 9, 11, 12	3, 14	1, 16	8	14
f_{shift}	Shift Frequency	150		150		150		MHz	4, 6, 9, 11, 12	3, 14	1, 16	8	14