



Integrated Device Technology, Inc.

FAST CMOS 18-BIT REGISTERED TRANSCEIVER

IDT54/74FCT16501AT/CT/ET
IDT54/74FCT162501AT/CT/ET
IDT54/74FCT162H501AT/CT/ET

FEATURES:

• Common features:

- 0.5 MICRON CMOS Technology
- **High-speed, low-power CMOS replacement for ABT functions**
- **Typical tsk(o) (Output Skew) < 250ps**
- **Low input and output leakage $\leq 1\mu\text{A}$ (max.)**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C

• Features for FCT16501AT/CT/ET:

- High drive outputs (-32mA IOH, 64mA IOL)
- Power off disable outputs permit "live insertion"
- Typical VOLP (Output Ground Bounce) < 1.0V at VCC = 5V, TA = 25°C

• Features for FCT162501AT/CT/ET:

- Balanced Output Drivers: $\pm 24\text{mA}$ (commercial), $\pm 16\text{mA}$ (military)
- Reduced system switching noise
- Typical VOLP (Output Ground Bounce) < 0.6V at VCC = 5V, TA = 25°C

• Features for FCT162H501AT/CT/ET:

- Bus Hold retains last active bus state during 3-state
- Eliminates the need for external pull up resistors

CMOS technology. These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch enable (LEAB and LEBA) and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. OEAB is the output enable for the B port. Data flow from the B port to the A port is similar but requires using OEBA, LEBA and CLKBA. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16501AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

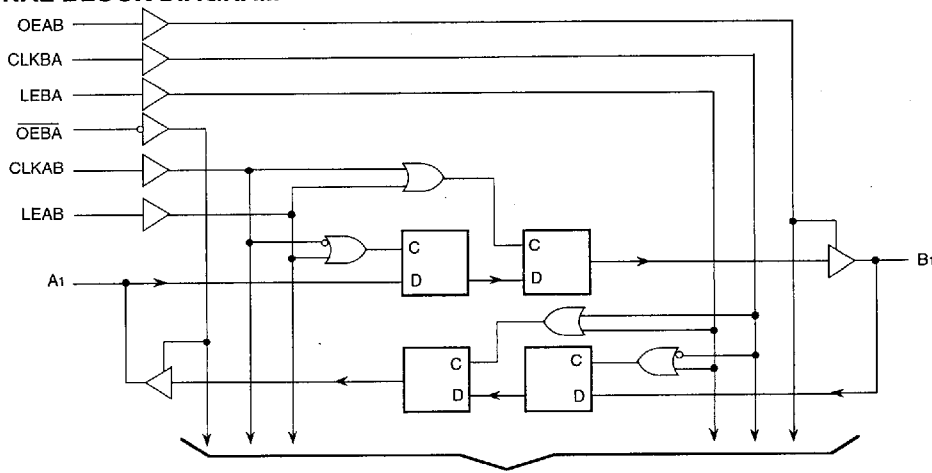
The FCT162501AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162501AT/CT/ET are plug-in replacements for the FCT16501AT/CT/ET and ABT16501 for on-board bus interface applications.

The FCT162H501AT/CT/ET have "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

DESCRIPTION:

The FCT16501AT/CT/ET and FCT162501AT/CT/ET 18-bit registered transceivers are built using advanced dual metal

FUNCTIONAL BLOCK DIAGRAM



TO 17 OTHER CHANNELS

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

2547 drw 01

MILITARY AND COMMERCIAL TEMPERATURE RANGES

JUNE 1996

©1996 Integrated Device Technology, Inc.

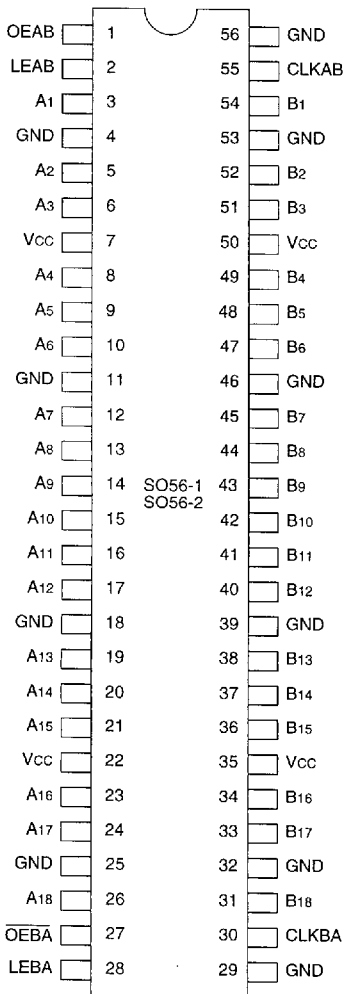
5.10

2547/7

1

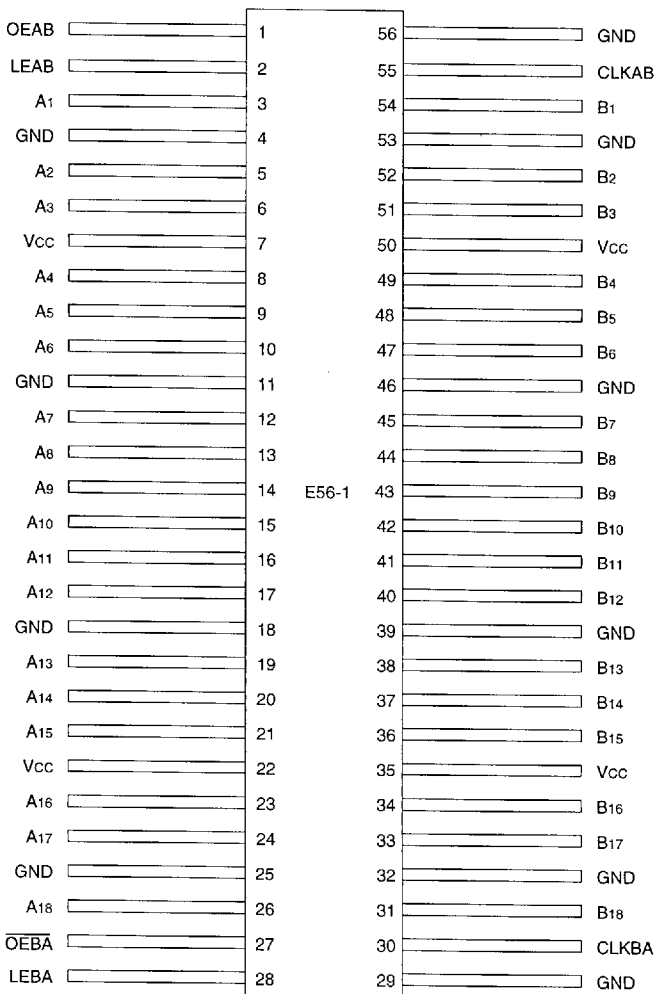
4825771 0023026 854

PIN CONFIGURATIONS



**SSOP
TSSOP
TOP VIEW**

2547 drw 02



**CERPACK
TOP VIEW**

2547 drw 03

5

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
\overline{OEBA}	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾

NOTE: 2547 tbl 01
1. On FCT16xH501T these pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc +0.5	-0.5 to Vcc +0.5	V
TA	Operating Temperature	-40 to +85	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	-60 to +120	-60 to +120	mA

- NOTES:** 2547 lmk 03
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
 - All device terminals except FCT162XXXT Output and I/O terminals.
 - Output and I/O terminals for FCT162XXXT.

FUNCTION TABLE^(1,4)

Inputs				Outputs	
OEAB	LEAB	CLKAB	Ax	Bx	
L	X	X	X	Z	
H	H	X	L	L	
H	H	X	H	H	
H	L	↑	L	L	
H	L	↑	H	H	
H	L	L	X	B ⁽²⁾	
H	L	H	X	B ⁽³⁾	

- NOTES:** 2547 tbl 02
- A-to-B data flow is shown. B-to-A data flow is similar but uses \overline{OEBA} , LEBA, and CLKBA.
 - Output level before the indicated steady-state input conditions were established.
 - Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
 - H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-impedance
↑ = LOW-to-HIGH Transition

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6.0	pF
	I/O Capacitance	VOUT = 0V	3.5	8.0	pF

- NOTE:** 2547 lmk 04
- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (STANDARD PARTS)

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	V _{CC} = Max.	V _I = V _{CC}	—	—	±1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾		—	—	±1		
I _{IL}	Input LOW Current (Input pins) ⁽⁵⁾		V _I = GND	—	—	±1	
	Input LOW Current (I/O pins) ⁽⁵⁾		—	—	±1		
I _{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	V _{CC} = Max.	V _O = 2.7V	—	—	±1	μA
I _{OZL}			V _O = 0.5V	—	—	±1	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾		-80	-140	-225	mA
V _H	Input Hysteresis	—		—	100	—	mV
I _{CC1}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}		—	5	500	μA
I _{CCH}							
I _{CCZ}							

2547 Ink 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16501T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _O	Output Drive Current	V _{CC} = Max., V _O = 2.5V ⁽³⁾		-50	—	-180	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3mA	2.5	3.5	—	V
			I _{OH} = -12mA MIL.	2.4	3.5	—	V
			I _{OH} = -15mA COM'L.	—	—	—	—
			I _{OH} = -24mA MIL. I _{OH} = -32mA COM'L. ⁽⁴⁾	2.0	3.0	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48mA MIL. I _{OL} = 64mA COM'L.	—	0.2	0.55	V
I _{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	V _{CC} = 0V, V _{IN} or V _O ≤ 4.5V		—	—	±1	μA

2547 Ink 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162501T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		60	115	200	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		-60	-115	-200	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -16mA MIL.	2.4	3.3	—	V
			I _{OH} = -24mA COM'L.	—	—	—	—
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 16mA MIL. I _{OL} = 24mA COM'L.	—	0.3	0.55	V

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is ±5μA at T_A = -55°C.

2547 Ink 07

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS HOLD)

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = -40°C to +85°C, Vcc = 5.0V ± 10%; Military: TA = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter		Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level		Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level		Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current ⁽⁴⁾	Standard Input ⁽⁵⁾	Vcc = Max.	Vi = Vcc	—	—	±1	μA
		Standard I/O ⁽⁵⁾			—	—	±1	
		Bus Hold Input			—	—	±100	
		Bus Hold I/O			—	—	±100	
I _{IL}	Input LOW Current ⁽⁴⁾	Standard Input ⁽⁵⁾	Vcc = Max.	Vi = GND	—	—	±1	
		Standard I/O ⁽⁵⁾			—	—	±1	
		Bus Hold Input			—	—	±100	
		Bus Hold I/O			—	—	±100	
I _{BHH}	Bus Hold Sustain Current ⁽⁴⁾	Bus Hold Input	Vcc = Min.	Vi = 2.0V	-50	—	—	μA
I _{BHL}			Vi = 0.8V	+50	—	—		
I _{OZH}	High Impedance Output Current		Vcc = Max.	Vo = 2.7V	—	—	±1	μA
I _{OZL}	(3-State Output pins) ^(5,6)			Vo = 0.5V	—	—	±1	
V _{IK}	Clamp Diode Voltage		Vcc = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current		Vcc = Max., Vo = GND ⁽³⁾		-80	-140	-225	mA
V _H	Input Hysteresis		—		—	100	—	mV
I _{CCL}	Quiescent Power Supply Current		Vcc = Max., Vi = GND or Vcc		—	5	500	μA
I _{CCH}								
I _{CCZ}								

2547 Ink 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Pins with Bus Hold are identified in the pin description.
5. The test limit for this parameter is ± 5μA at TA = -55°C.
6. Does not include Bus Hold I/O pins.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$	—	0.5	1.5	mA	
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open $OEAB = \overline{OEBA} = V_{CC}$ or GND One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	75	120 $\mu A/$ MHz	
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ (CLKAB) 50% Duty Cycle $OEAB = \overline{OEBA} = V_{CC}$ $LEAB = \text{GND}$ One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.3	3.2	
		$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ (CLKAB) 50% Duty Cycle $OEAB = \overline{OEBA} = V_{CC}$ $LEAB = \text{GND}$ Eighteen Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	6.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	8.5	20.8 ⁽⁵⁾	

NOTES:

2547 tbl 09

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} \text{DHNT} + I_{CCD} (f_{CP}N_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current} (I_{CC1}, I_{CC2} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input} (V_{IN} = 3.4V)$
 $\text{DH} = \text{Duty Cycle for TTL Inputs High}$
 $\text{NT} = \text{Number of TTL Inputs at DH}$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$



SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT16501AT/162501AT				FCT16501CT/162501CT				FCT16501ET/162501ET				Unit	
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.			
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.		
f _{MAX}	CLKAB or CLKBA frequency ⁽⁴⁾	CL = 50pF	—	150	—	150	—	150	—	150	—	150	—	—	MHz	
t _{PLH}	Propagation Delay Ax to Bx or Bx to Ax	RL = 500Ω	1.5	5.1	1.5	5.6	1.5	4.6	1.5	4.6	1.5	3.8	—	—	ns	
t _{PLH}	Propagation Delay LEBA to Ax, LEAB to Bx		1.5	5.6	1.5	6.0	1.5	5.3	1.5	5.6	1.5	4.2	—	—	ns	
t _{PLH}	Propagation Delay CLKBA to Ax, CLKAB to Bx		1.5	5.6	1.5	6.0	1.5	5.3	1.5	5.4	1.5	4.2	—	—	ns	
t _{PZH}	Output Enable Time OEBA to Ax, OEAB to Bx		1.5	6.0	1.5	6.4	1.5	5.6	1.5	6.0	1.5	4.8	—	—	ns	
t _{PHZ}	Output Disable Time OEBA to Ax, OEAB to Bx		1.5	5.6	1.5	6.0	1.5	5.2	1.5	5.6	1.5	5.2	—	—	ns	
t _{SU}	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA		3.0	—	3.0	—	3.0	—	3.0	—	2.4	—	—	—	ns	
t _H	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		0	—	0	—	0	—	0	—	0	—	—	—	ns	
t _{SU}	Set-up Time HIGH or LOW Ax to LEAB, Bx to LEBA		Clock LOW	3.0	—	3.0	—	3.0	—	3.0	—	2.0	—	—	—	ns
			Clock HIGH	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	—	—	ns
t _H	Hold Time, HIGH or LOW Ax to LEAB, Bx to LEBA		1.5	—	1.5	—	1.5	—	1.5	—	0.5	—	—	—	ns	
t _W	LEAB or LEBA Pulse Width HIGH ⁽⁴⁾		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	—	—	ns	
t _W	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽⁴⁾		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	—	—	ns	
t _{SK(o)}	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns	

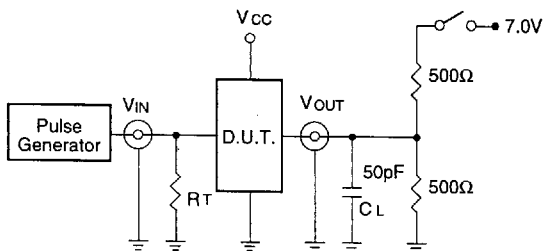
NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

2547 tbi 10

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2547 drw 04

SWITCH POSITION

Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

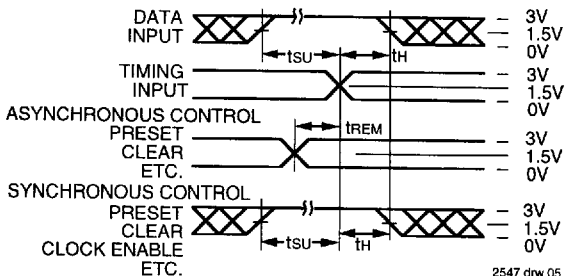
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

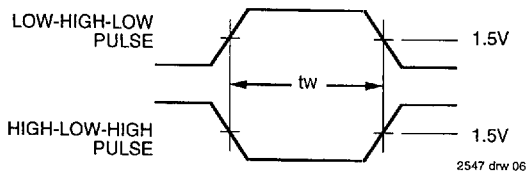
2547 Ink 11

SET-UP, HOLD AND RELEASE TIMES



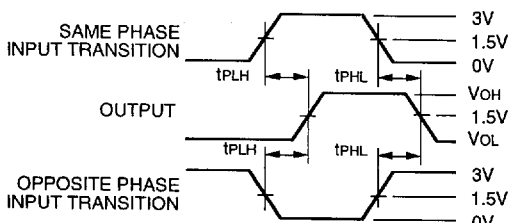
2547 drw 05

PULSE WIDTH



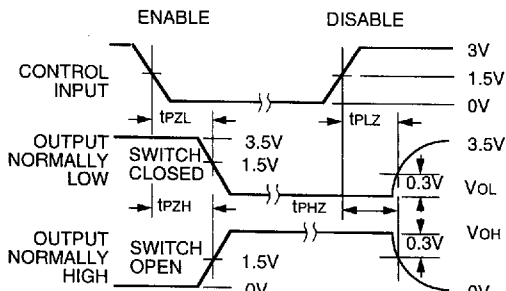
2547 drw 06

PROPAGATION DELAY



2547 drw 07

ENABLE AND DISABLE TIMES

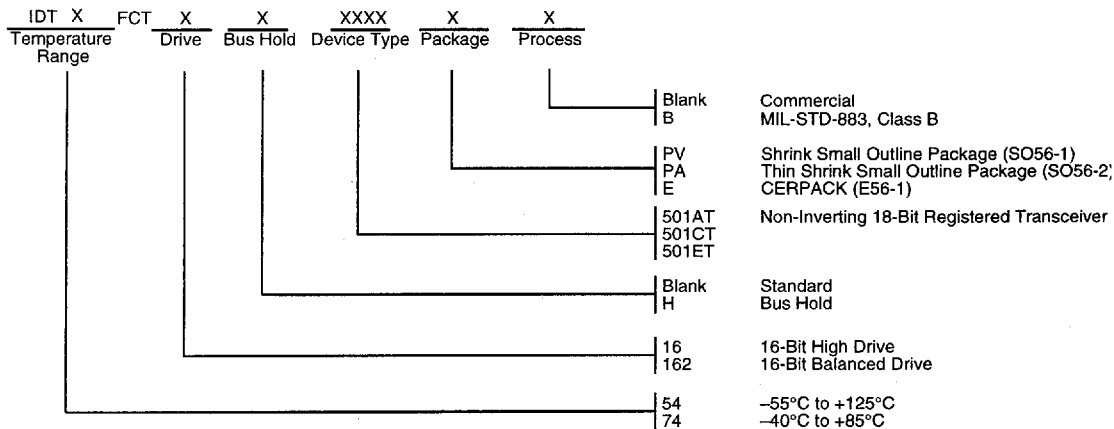


2547 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION



2547 drw 09