CMOS NAND GATES

High-Voltage Types (20-Volt Rating)

Quad 2 Input — CD4011B
Dual 4 Input — CD4012B
Triple 3 Input — CD4023B

■ CD4011B, CD4012B, and CD4023B NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of CMOS gates. All inputs and outputs are buffered.

The CD4011B, CD4012B, and CD4023B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead dual-in-line small-outline plastic package (M suffix), thin shrink small-outline package (PWR suffix), 14-lead small-outline package (NSR suffix), and in chip form (H suffix).

Features:

■ Propagation delay time = 60 ns (typ.) at $C_L = 50$ pF, $V_{DD} = 10$ V
■ Buffered inputs and outputs
■ Standardized symmetrical output characteristics
■ Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
■ 100% tested for quiescent current at 20 V
■ 5-V, 10-V, and 15-V parametric ratings
■ Noise margin (over full package temperature range:

  1 V at $V_{DD} = 5$ V
  2 V at $V_{DD} = 10$ V
  2.5 V at $V_{DD} = 15$ V

■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"

CD4011B
FUNCTIONAL DIAGRAM
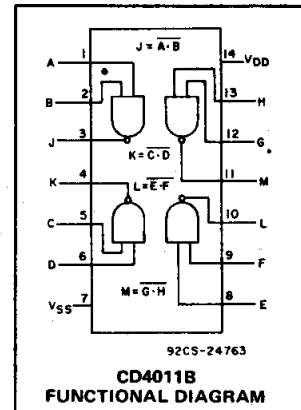
MAXIMUM RATINGS, *Absolute-Maximum Values:*
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) .... –0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... –0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
  For T_A = –55°C to +100°C 500mW
  For T_A = +100°C to +125°C............................... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE–TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A).. –55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}).. –65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C
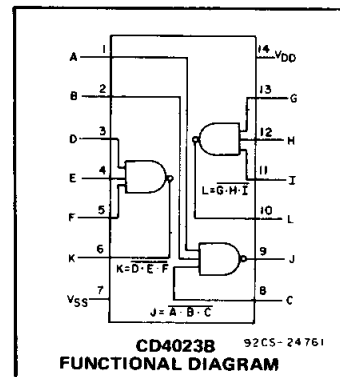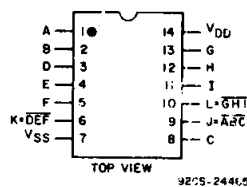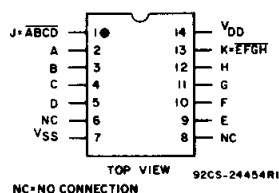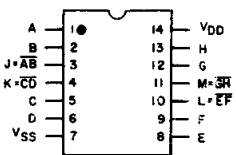

CD4012B
FUNCTIONAL DIAGRAM
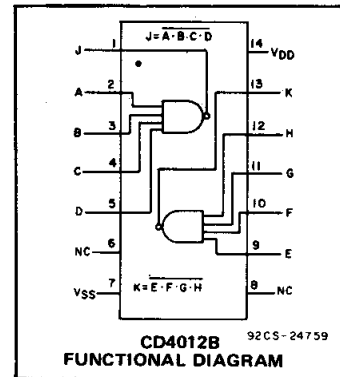
RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

CD4023B
FUNCTIONAL DIAGRAM

TERMINAL ASSIGNMENTS

CD4011B

CD4012B

NC-NO CONNECTION

CD4023B

CD4011B, CD4012B, CD4023B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTER-ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)				+25			UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	µA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1.5				—	—	1.5	V
	9	–	10	3				—	—	3	
	13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	—	—	
	1,9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	±10^{-5}	±0.1	µA
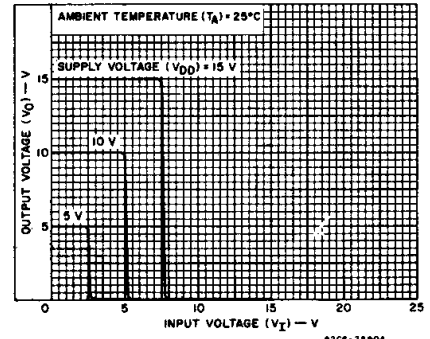
Fig.1 — Typical voltage transfer characteristics.
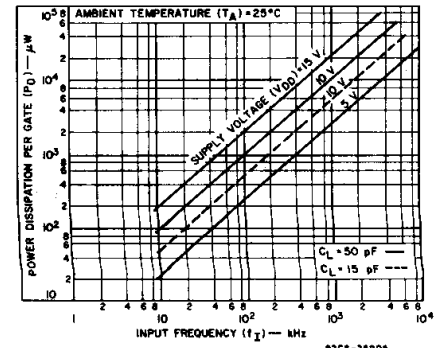
Fig.2 — Typical power dissipation characteristics.

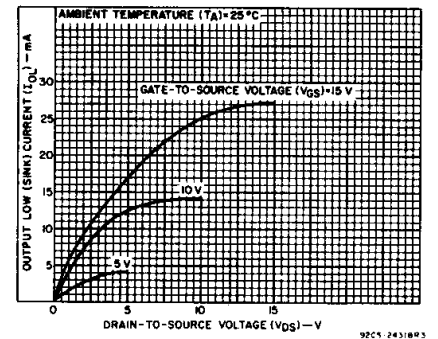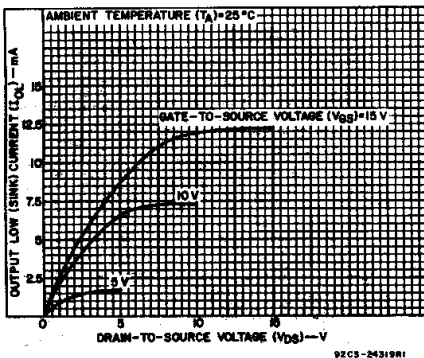
Fig.3 — Typical output low (sink) current characteristics.

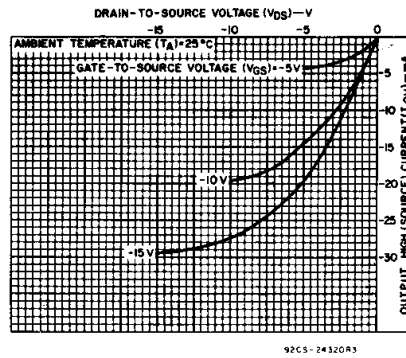
Fig.4 — Minimum output low (sink) current characteristics.

Fig.5 — Typical output high (source) current characteristics.
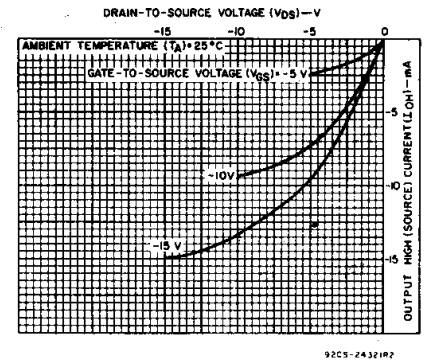

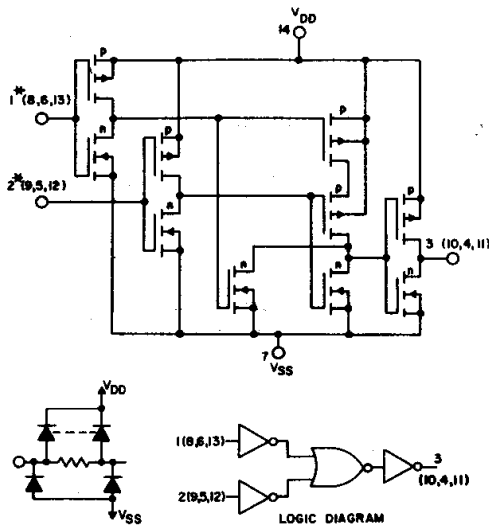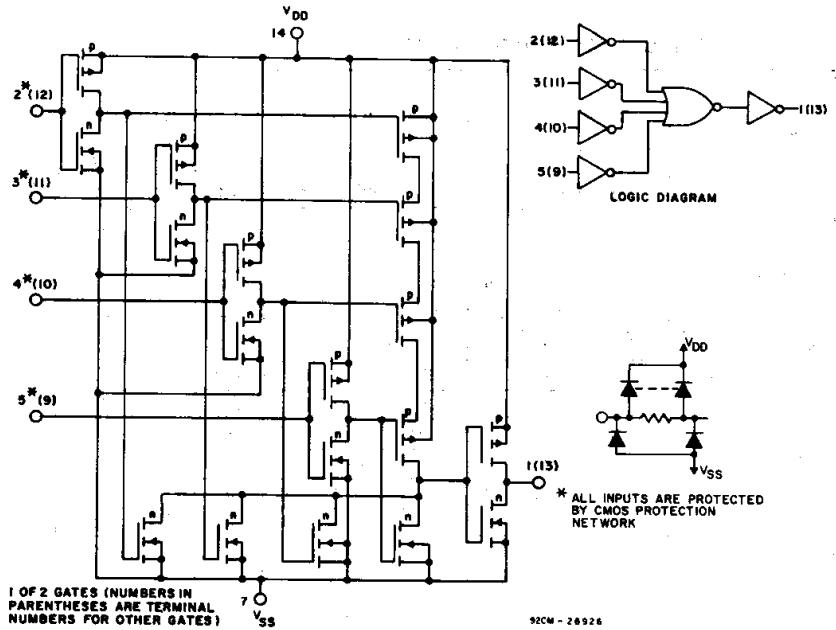Fig.6 — Minimum output high (source) current characteristics.

Fig.7 – Schematic and logic diagrams for CD4011B.

Fig.8 – Schematic and logic diagrams for CD4012B.
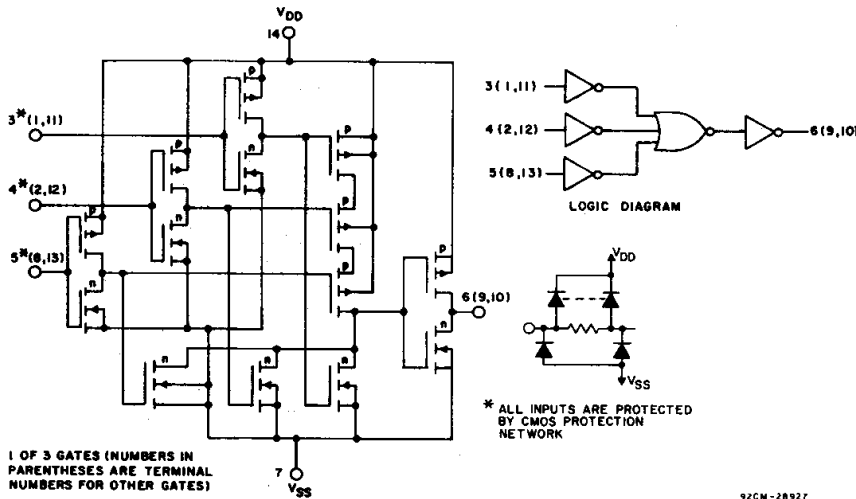
Fig. 9 – Schematic and logic diagrams for CD4023B.
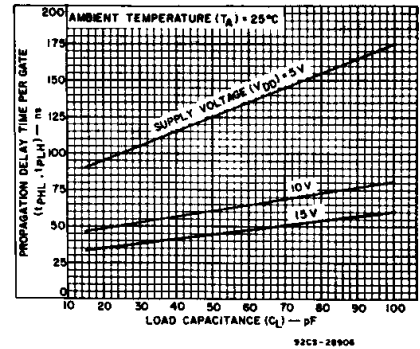
Fig.10 – Typical propagation delay time per gate as a function of load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$; Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
	V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}	5	125	250	ns
	10	60	120	
	15	45	90	
Transition Time, t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF
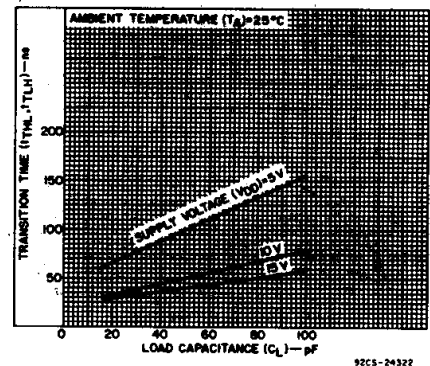
Fig.11 – Typical transition time as a function of load capacitance.
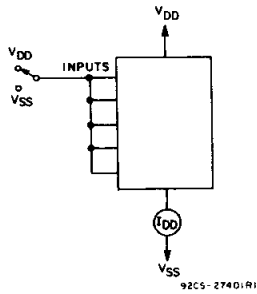
Fig.12 — Quiescent-device-current test circuit.
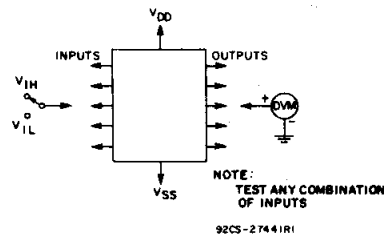
Fig.13 — Input-voltage test circuit.
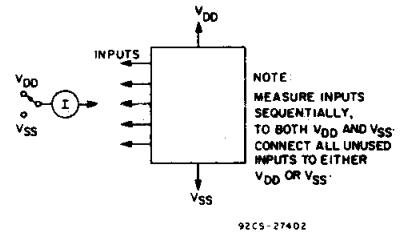
Fig.14 — Input-current test circuit.

Chip Dimensions and Pad Layouts

42-50
(1.067-1.270)

4-10
(0.102-0.254)

61-69
(1.549-1.752)

92CS-35052

CD4011BH

57-65
(1.448-1.651)

4-10
(0.102-0.254)

66-74
(1.667-1.879)

92CS-28683

CD4012BH

57-65
(1.448-1.651)

4-10
(0.102-0.254)

66-74
(1.667-1.879)

92CS-35061
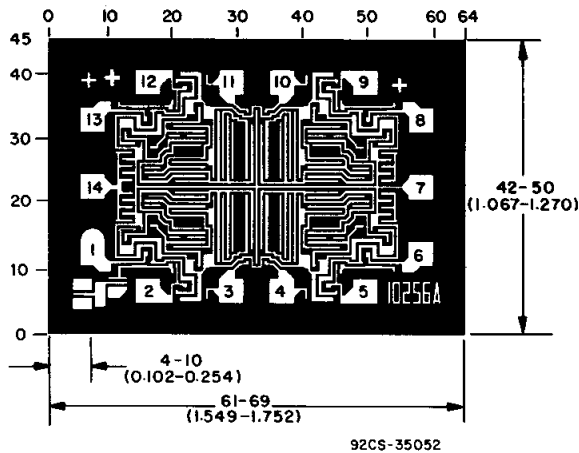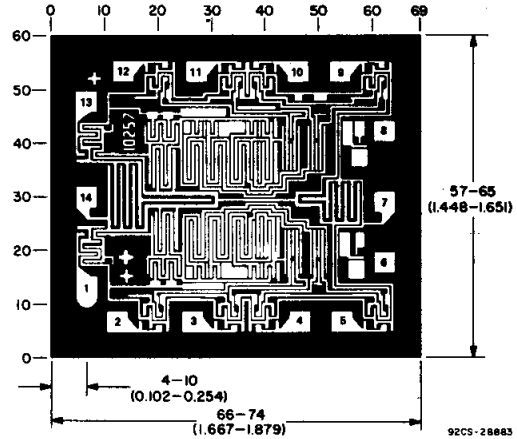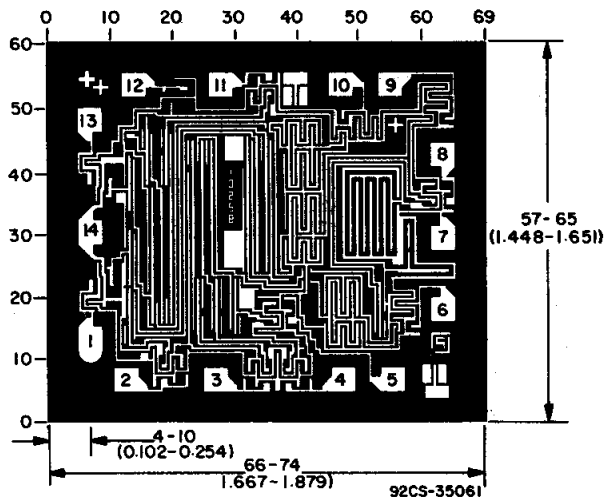
CD4023BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.' Grid graduations are in mils (10^{-3} inch).

3

COMMERCIAL CMOS HIGH VOLTAGE ICs

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Product Folder: CD4011B, CMOS Quad 2-Input NAND Gate

PRODUCT FOLDER | PRODUCT INFO: FEATURES | DESCRIPTION | DATASHEETS | PRICING/AVAILABILITY/PKG | SAMPLES
| APPLICATION NOTES | USER GUIDES | MORE LITERATURE

PRODUCT SUPPORT: TRAINING

CD4011B, CMOS Quad 2-Input NAND Gate
DEVICE STATUS: **ACTIVE**

PARAMETER NAME	CD4011B
Voltage Nodes (V)	5, 10, 15
Vcc range (V)	3 to 18
No. of Gates	4

FEATURES   ▲Back to Top

- Propagation delay time = 60ns (typ.) at C_L = 50 pF, V_{DD} = 10 V
- Buffered inputs and outputs
- Standardized symmetrical output characteristics
- Maximum input current of 1 uA at 18 V over-full package temperature range; 100 nA at 18 V and 25°C
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin (over full package temperature range:
     1 V at V_{DD} = 5 V
     2 V at V_{DD} = 10 V
     2.5 at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"

Quad 2 Input—CD4011B
Dual 4 Input—CD4012B
Triple 3 Input—CD4023B

DESCRIPTION   ▲Back to Top

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TECHNICAL DOCUMENTS   ▲Back to Top
To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET   ▲Back to Top
Full datasheet in Acrobat PDF: cd4011b.pdf (202 KB,Rev.B) (Updated: 05/03/2002)

APPLICATION NOTES   ▲Back to Top
View Application Notes for Digital Logic

- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Understanding Buffered and Unbuffered CD4xxxB Series Device Characteristics (SCHA004 - Updated: 12/03/2001)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)

Product Folder: CD4011B, CMOS Quad 2-Input NAND Gate

- **Enhanced Plastic Portfolio Brochure** (SGZB004, 387 KB - Updated: 08/19/2002)
- **Logic Reference Guide** (SCYB004, 1032 KB - Updated: 10/23/2001)
- **MicroStar Junior BGA Design Summary** (SCET004, 167 KB - Updated: 07/28/2000)
- **Military Brief** (SGYN138, 803 KB - Updated: 10/10/2000)
- **Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A)** (SDYZ001A, 138 KB - Updated: 07/01/1996)
- **Palladium Lead Finish User's Manual** (SDYV001, 2041 KB - Updated: 11/01/1996)
- **QML Class V Space Products Military Brief (Rev. A)** (SGZN001A, 257 KB - Updated: 10/07/2002)

- **LOGIC Pocket Data Book** (SCYD013, 4837 KB - Updated: 12/05/2002)
- **Signal Switch Data Book** (SCDD003, 10259 KB - Updated: 03/19/2001)

ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (ºC)	STATUS	DSCC NUMBER	PRODUCT CONTENT	SAMPLES
CD4011BE	PDIP (N)	14	-55 TO 125	ACTIVE		View Product Content	Request Samples
CD4011BM	SOIC (D)	14	-55 TO 125	ACTIVE		View Product Content	Request Samples
CD4011BNSR	SOP (NS)	14	-55 TO 125	ACTIVE		View Product Content	Request Samples
CD4011BPWR	TSSOP (PW)	14	-55 TO 125	ACTIVE		View Product Content	Request Samples

DEVICE INFORMATION
Updated Daily

ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (ºC)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY
89265AKB3T	OBSOLETE	(WR) | 14	-55 TO 125		View Contents	1KU |	
CD4011BE	ACTIVE	PDIP (N) | 14	-55 TO 125		View Contents	1KU | 0.12	25
CD4011BF	ACTIVE	CDIP (J) | 14	-55 TO 125		View Contents	1KU | 2.25	1

TI INVENTORY STATUS
As Of 08:00 AM GMT, 17 Apr 2003

IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME
0*		Call**
0*	>10k | 28 Apr	4 WKS
3850*	1000 | 12 May	8 WKS
	>10k | 20 May	

REPORTED DISTRIBUTOR INVENTORY
As Of 08:00 AM GMT, 17 Apr 2003

DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
None Reported View Distributors		
Avnet | Americas	>1k	BUY NOW
EBV Electronik | Europe	>1k	BUY NOW
Avnet-SILICA | Europe	>1k	BUY NOW
DigiKey | Americas	>1k	BUY NOW
Newark Electronics | Americas	>1k	BUY NOW
Avnet-SILICA | Europe	277	BUY NOW
Avnet | Americas	113	BUY NOW

Product Folder: CD4011B, CMOS Quad 2-Input NAND Gate

Part	Status	Package	Pin	Temp	Contents	1KU	Price	MSL	Avail	Qty	Date	Lead	Distributor	Region	Stock	Buy
CD4011BF3A	ACTIVE	CDIP (J)	14	-55 TO 125	View Contents	1KU	2.57	1	>10k*	132	29 Apr	8 WKS	EBV Electronik	Europe	350	BUY NOW
										100	19 May		Avnet	Americas	272	BUY NOW
										>10k	20 May					
CD4011BK3	OBSOLETE	(WR)	14	-55 TO 125	View Contents	1KU			0*			Call**	None Reported View Distributors			
CD4011BM	ACTIVE	SOIC (D)	14	-55 TO 125	View Contents	1KU	0.08	50	7850*	>10k	12 May	2 WKS	EBV Electronik	Europe	>1k	BUY NOW
													Avnet	Americas	>1k	BUY NOW
													DigiKey	Americas	>1k	BUY NOW
													Newark Electronics	Americas	453	BUY NOW
													Avnet-SILICA	Europe	100	BUY NOW
CD4011BM96	ACTIVE	SOIC (D)	14	-55 TO 125	View Contents	1KU	0.08	2500	0*	>10k	16 Apr	2 WKS	Avnet	Americas	>1k	BUY NOW
													EBV Electronik	Europe	>1k	BUY NOW
													DigiKey	Americas	>1k	BUY NOW
CD4011BNSR	ACTIVE	SOP (NS)	14	-55 TO 125	View Contents	1KU	0.27	2000	0*	943	21 Apr	4 WKS	DigiKey	Americas	>1k	BUY NOW
										>10k	08 May					
CD4011BPW	ACTIVE	TSSOP (PW)	14	-55 TO 125	View Contents	1KU	0.17	90	0*	2430	16 Apr	4 WKS	None Reported View Distributors			
										>10k	08 May					
CD4011BPWR	ACTIVE	TSSOP (PW)	14	-55 TO 125	View Contents	1KU	0.08	2000	0*	1681	21 Apr	4 WKS	DigiKey	Americas	>1k	BUY NOW
										>10k	08 May					
JM38510/05051BCA	ACTIVE	CDIP (J)	14	-55 TO 125	View Contents	1KU	15.06	1	221*	796	05 May	8 WKS	Avnet	Americas	32	BUY NOW
										1023	12 May		Avnet-SILICA	Europe	1	BUY NOW
										>10k	20 May					

Table Data Updated on: 4/17/2003