



FEATURES/BENEFITS

- 5V tolerant inputs and outputs
- $10\mu\text{A}$ I_{CCQ} quiescent power supply current
- Hot insertable
- 2.0V–3.6V V_{CC} supply operation
- $\pm 24\text{mA}$ balanced output drive
- Power down high impedance inputs and outputs
- $t_{\text{PD}} = 4.1\text{ns}$ max.
- Input hysteresis for noise immunity
- Meets or exceeds JEDEC Standard 36 specifications
- Multiple power and ground pins for low noise
- Operating temperature range:
–40°C to 85°C
- Latch-up performance exceeds 500mA
- ESD performance:
Human body model > 2000V
Machine model > 200V
- Packages available:
48-pin TSSOP
48-pin SSOP

DESCRIPTION

The QS74LVC16244A is a 16-bit bus interface buffer with three-state output that is ideal for driving address, clocks, and data buses. Output enables are used to enable or disable Y ports by placing them in a high impedance condition. The 3.3V LVC family features low power, low switching noise, and fast switching speeds for low power portable applications as well as high-end, advanced workstation applications. 5V tolerant inputs and outputs allow these LVC products to be used in mixed 5V and 3.3V applications. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. To accommodate hot-plug or live insertion applications, this product is designed not to load an active bus when V_{CC} is removed. However, during power up or power down sequence, $\overline{\text{OE}}$ should be tied to V_{CC} to ensure high-impedance state on the outputs.

Figure 1. Functional Block Diagram

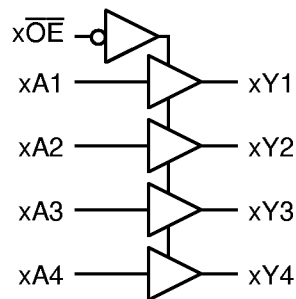


Figure 2. Pin Configuration
(All Pins Top View)

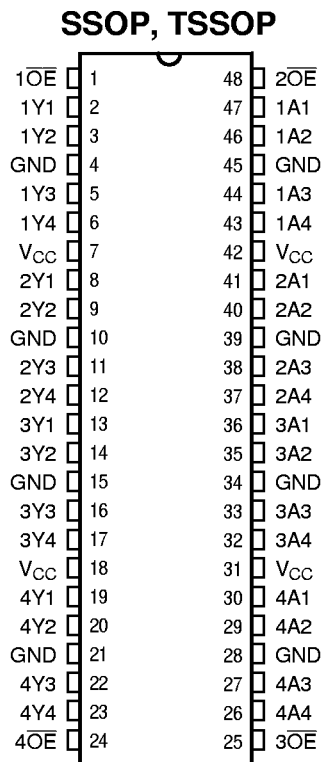


Table 1. Pin Description

Name	Description
\overline{xOE}	Three-State Output Enable Inputs
xAx	Data Inputs (Bus Hold)
xYx	Three-State Outputs

Table 2. Function Table

Inputs		Outputs
\overline{xOE}	xAx	xYx
L	L	L
L	H	H
H	X	Hi-Z

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to 7.0V
DC Output Voltage V_{OUT}	
Outputs HIGH-Z	-0.5V to 7.0V
Outputs Active	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage V_{IN}	-0.5V to 7.0V
DC Input Diode Current with $V_{IN} < 0$	-50mA
DC Output Diode Current	
$V_O < 0$	-50mA
$V_O > V_{CC}$	50mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	$\pm 50mA$
DC Supply Current per Supply Pin	$\pm 100mA$
DC Ground Current per Ground Pin	$\pm 100mA$
T_{STG} Storage Temperature	-65°C to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 4. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit	
V _{CC}	Supply Voltage, Operating	2.0	3.6	V	
	Supply Voltage, Data Retention Only	1.5	3.6		
V _{IH}	Input HIGH Voltage	2.0	—	V	
V _{IL}	Input LOW Voltage	—	0.8	V	
V _{IN}	Input Voltage	0	5.5	V	
V _{OUT}	Output Voltage in Active State	0	V _{CC}	V	
	Output Voltage in "OFF" State	0	5.5		
I _{OH}	Output Current HIGH	V _{CC} = 3.0–3.6V	—	–24	mA
		V _{CC} = 2.7V	—	–12	
I _{OL}	Output Current LOW	V _{CC} = 3.0–3.6V	—	24	mA
		V _{CC} = 2.7V	—	12	
Δt/Δv	Input Transition Slew Rate	—	10	ns/V	
T _A	Operating Free Air Temperature	–40	85	°C	

Table 5. DC Electrical Characteristics Over Operating Range

Industrial Temperature Range, T_A = –40°C to 85°C

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.7V, I _{OH} = –100μA	V _{CC} – 0.2	—	—	V
		V _{CC} = 2.7V, I _{OH} = –12mA	2.2	—	—	
		V _{CC} = 3.0V, I _{OH} = –12mA	2.4	—	—	
		V _{CC} = 3.0V, I _{OH} = –24mA	2.2	—	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.7V, I _{OL} = 100μA	—	—	0.2	V
		V _{CC} = 2.7V, I _{OL} = 12mA	—	—	0.4	
		V _{CC} = 3.0V, I _{OL} = 24mA	—	—	0.55	
V _{IK}	Input Clamp Voltage	V _{CC} = 2.7V, I _{IN} = –18mA	—	–0.7	–1.2	V
I _I	Input Leakage Current	V _I = 0V, V _I = 5.5V, V _{CC} = 3.6V	—	—	±1.0	μA
I _{OZ}	High-Z I/O Leakage	V _O = 0V, V _O = 5.5V, V _I = V _{IH} or V _{IL} , V _{CC} = 3.6V	—	—	±1.0	μA
I _{OFF}	Power Off Leakage	V _{CC} = 0V, V _I or V _O = 5.5V	—	—	10	μA
I _{CC}	Quiescent Power Supply Current	V _{CC} = 3.6V, V _{IN} = V _{CC} or GND	—	0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current per Inputs at TTL HIGH	V _{CC} = 3.6V, V _{IN} = V _{CC} – 0.6V ⁽²⁾	—	2.0	3.0	μA

Notes:

1. Typical values are at V_{CC} = 3.3V and T_A = 25°C.
2. Per TTL driven input. All other inputs at V_{CC} or GND.

Table 6. Dynamic Switching Characteristics

Symbol	Parameter	Test Conditions		Typ ⁽¹⁾	Unit
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50pF, V _{CC} = 3.3V	V _{IH} = 3.3V, V _{IL} = 0V	0.8	V
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50pF, V _{CC} = 3.3V	V _{IH} = 3.3V, V _{IL} = 0V	0.8	V
C _{PD}	Power Dissipation	C _L = 50pF, f = 10MHz, V _{CC} = 3.3 ±0.3V	Output Enable	20	pF
			Output Disable	4	

Note:

1. Typical values are at V_{CC} = 3.3V, 25°C ambient.

Table 7. Capacitance⁽¹⁾

Symbol	Pins	Conditions	Typ	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V, V _{OUT} = 0V, f = 1MHz	7.0	pF
C _{I/O}	I/O Capacitance	V _{IN} = 0V, V _{OUT} = 0V, f = 1MHz	8.0	pF

Note:

1. Capacitance is characterized but not production tested.

Table 8. Switching Characteristics Over Operating Range

Industrial Temperature Range, T_A = -40°C to 85°C.

C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

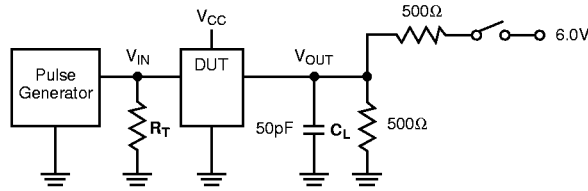
Symbol	Description ⁽¹⁾	V _{CC} = 3.3 ±0.3V		V _{CC} = 2.7V ⁽²⁾		Unit
		Min	Max	Min	Max	
t _{PD}	Propagation Delay xAx to xYx	1.5	4.1	1.5	4.7	ns
t _{EN}	Output Enable Time xOE to xYx	1.5	4.6	1.5	5.8	ns
t _{DIS}	Output Disable Time ⁽²⁾ xOE to xYx	1.5	5.8	1.5	6.2	ns
t _{SK(O)}	Output Skew ⁽³⁾	—	0.5	—	—	ns

Notes:

1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.
2. Guaranteed by characterization.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by characterization but not production tested.

TEST CIRCUIT AND WAVEFORMS

Figure 3. Test Circuit



SWITCH POSITION	
Test	Switch
Open Drain	
Disable LOW	6V
Enable LOW	
Disable HIGH	GND
Enable HIGH	
All Other Inputs	Open

DEFINITIONS:
 C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

Figure 4. Setup, Hold, and Release Timing

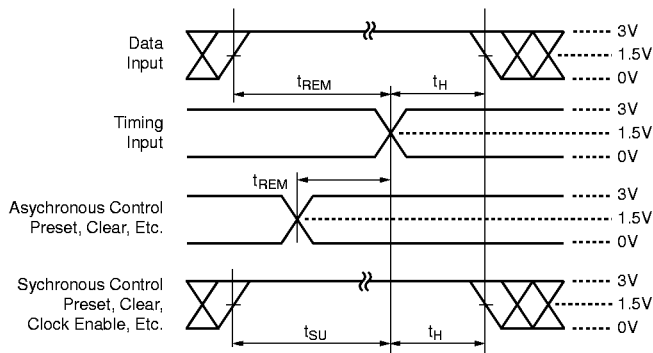


Figure 6. Pulse Width

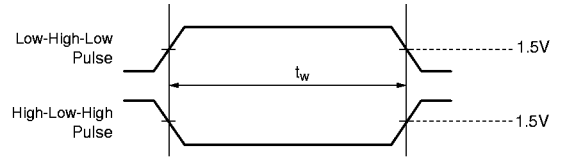
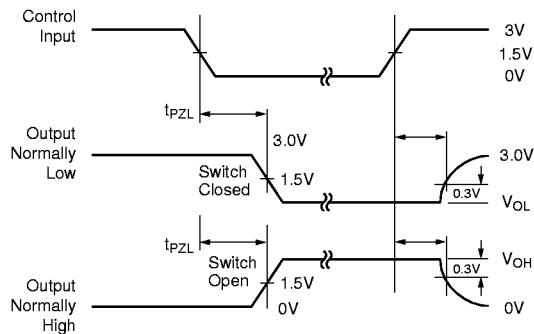
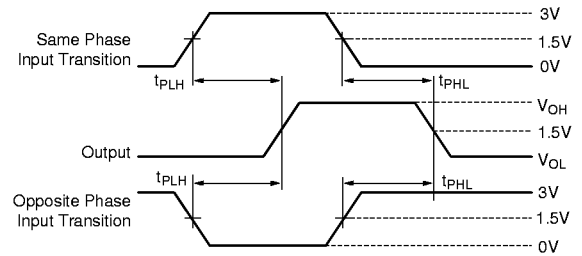


Figure 5. Enable and Disable Timing

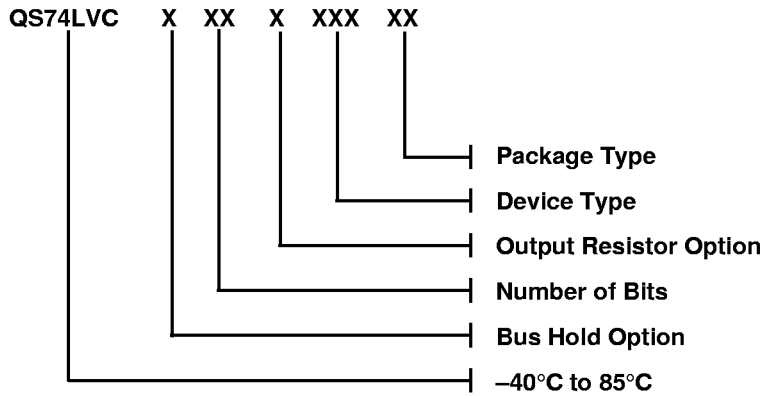


- Notes:
1. Input Control Enable = LOW and Input Control Disable = HIGH.
 2. Pulse Generator for All Pulses: Rate \leq 1.0MHz;
 $Z_{OUT} \leq 50\Omega$; $t_F, t_R \leq 2.5ns$.

Figure 7. Propagation Delay



ORDERING INFORMATION



Bus Hold Option:
Blank – No Bus Hold

Number of Bits:
16 – 16-Bit

Output Resistor Option:
Blank – No Output Resistor

Device Type:
244

Package Type:
PV – SSOP, 300 mil
PA – TSSOP, 240 mil