National Semiconductor

74VHC164
Serial-In, Parallel-Out Shift Register

General Description

The VHC164 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHC164 is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the Low-to-High transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs Low independent of the clock. An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

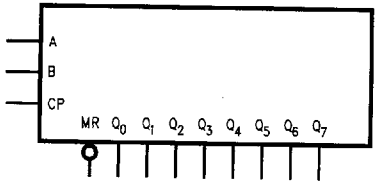
- Low power dissipation:
  I_{CC} = 4 μA (max) at T_A = 25°C
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
- All inputs are equipped with a power down protection function
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Low noise: V_{OLP} = 0.8V (max)
- Pin and function compatible with 74HC164

Ordering Code: See Section 6

Commercial	Package Number	Package Description
74VHC164M	M14A	14-Lead Molded JEDEC SOIC
74VHC164SJ	M14D	14-Lead Molded EIAJ SOIC
74VHC164MTC	MTC14	14-Lead Molded JEDEC Type 1 TSSOP
74VHC164N	N14A	14-Lead Molded DIP

Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

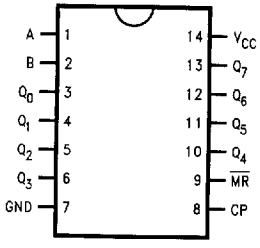


TL/F/11636–1

Pin Names	Description
A, B	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$	Master Reset Input (Active Low)
Q_0–Q_7	Outputs

Connection Diagram

Pin Assignment for DIP, TSSOP and SOIC



TL/F/11636–2

Functional Description

The VHC164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active High Enable for data entry through the other input. An unused input must be tied High.

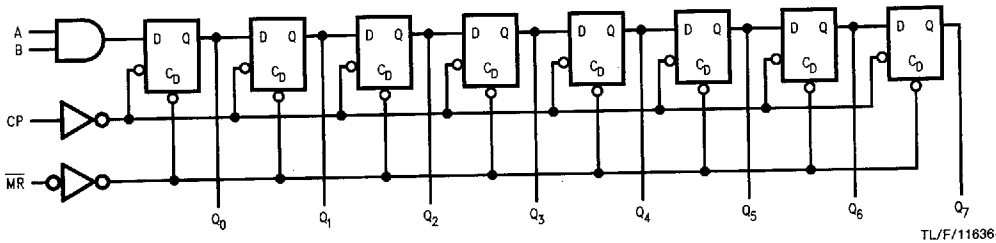
Each Low-to-High transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A Low level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs Low.

Function Table

Operating Mode	Inputs			Outputs	
	$\overline{MR}$	A	B	Q_0	Q_1–Q_7
Reset (Clear)	L	X	X	L	L–L
Shift	H	L	L	L	Q_0–Q_6
	H	L	H	L	Q_0–Q_6
	H	H	L	L	Q_0–Q_6
	H	H	H	H	Q_0–Q_6

H = High Voltage Levels
L = Low Voltage Levels
X = Immaterial
Q = Lower case letters indicate the state of the referenced input or output one setup time prior to the Low-to-High clock transition.

Logic Diagram



TL/F/11636–3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to + 7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
DC Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Note 1: *Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of circuits outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC					Units	Conditions	
			T_A = 25°C			T_A = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0	1.50			1.50		V		
		3.0–5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	Low Level Input Voltage	2.0			0.50		0.50	V		
		3.0–5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

DC Characteristics for 'VHC Family Devices: See Section 2 for Waveforms (Continued)

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$ Typ	74VHC $T_A = 25°C$ Limits	Units	Conditions	Fig. No.
*V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.5	0.8	V	C_L = 50 pF	2-11, 12
*V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.5	0.8	V	C_L = 50 pF	2-11, 12
*V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0		3.5	V	C_L = 50 pF	2-11, 12
*V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0		1.5	V	C_L = 50 pF	2-11, 12

*Parameter guaranteed by design.

AC Electrical Characteristics for 'VHC: See Section 2 for Waveforms

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$			74VHC $T_A = -40°C$ to $+85°C$		Units	Conditions	Fig. No.
			Min	Typ	Max	Min	Max			
f_{MAX}	Maximum Clock Frequency	3.3 ± 0.3	80	125		65		MHz	C_L = 15 pF	
			50	75		45			C_L = 50 pF	
		5.0 ± 0.5	125	175		105		MHz	C_L = 15 pF	
			85	115		75			C_L = 50 pF	
t_{PLH}, t_{PHL}	Propagation Delay Time ($CP-Q_n$)	3.3 ± 0.3		8.4	12.8	1.0	15.0	ns	C_L = 15 pF	2-5, 6
				10.9	16.3	1.0	18.5		C_L = 50 pF	2-5, 6
		5.0 ± 0.5		5.8	9.0	1.0	10.5	ns	C_L = 15 pF	2-5, 6
				7.3	11.0	1.0	12.5		C_L = 50 pF	2-5, 6
t_{PLH}, t_{PHL}	Propagation Delay Time ($\overline{MR}-Q_n$)	3.3 ± 0.3		8.3	12.8	1.0	15.0	ns	C_L = 15 pF	2-5, 6
				10.8	16.3	1.0	18.5		C_L = 50 pF	2-5, 6
		5.0 ± 0.5		5.2	8.6	1.0	10.0	ns	C_L = 15 pF	2-5, 6
				6.7	10.6	1.0	12.0		C_L = 50 pF	2-5, 6
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open	
C_{PD}	Power Dissipation Capacitance			76				pF	(Note 1)	

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}.

AC Operating Requirements for 'VHC: See Section 2 for Waveforms

Symbol	Parameter	*V_{CC} (V)	74VHC $T_A = 25°C$		74VHC $T_A = -40°C$ to $+85°C$	Units	Conditions	Fig. No.
			Typ	Guaranteed Minimum				
$t_{W(L)}$	Minimum Pulse Width (CP)	3.3		5.0	5.0	ns		2-6
$t_{W(H)}$		5.0		5.0	5.0			
$t_{W(L)}$	Minimum Pulse Width ($\overline{MR}$)	3.3		5.0	5.0	ns		2-6
		5.0		5.0	5.0			
t_S	Minimum Setup Time	3.3		5.0	6.0	ns		2-9
		5.0		4.5	4.5			
t_H	Minimum Hold Time	3.3		0.0	0.0	ns		2-9
		5.0		1.0	1.0			
t_{rem}	Minimum Removal Time ($\overline{MR}$)	3.3		2.5	2.5	ns		2-6, 9
		5.0		2.5	2.5			

*V_{CC} is 3.3 ±0.3V or 5.0 ±0.5V