

# TC74ACT32P/F/FN

## QUAD 2-INPUT OR GATE

The TC74ACT32 is an advanced high speed CMOS 2-INPUT OR GATE fabricated with silicon gate and double-layer metal wiring CMOS technology.

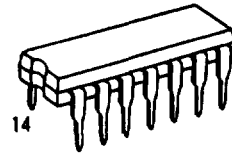
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

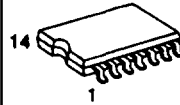
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### FEATURES:

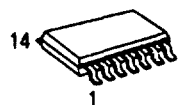
- High Speed .....  $t_{pd} = 4.5\text{ns}$  (typ.) at  $V_{CC} = 5\text{V}$
- Low Power Dissipation .....  $I_{CC} = 4\mu\text{A}$  (Max.) at  $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs .....  $V_{IL} = 0.8\text{V}$  (Max.)  
 $V_{IH} = 2.0\text{V}$  (Min.)
- Symmetrical Output Impedance ...  $|I_{OH}| = I_{OL} = 24\text{mA}$  (Min.)  
Capability of driving  $50\Omega$  transmission lines.
- Balanced Propagation Delays .....  $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74F32



P (DIP14-P-300)

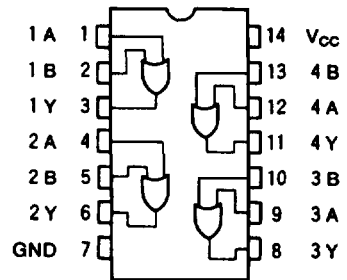


F (SOP14-P-300)



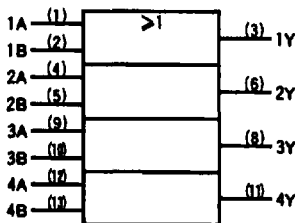
FN (SOL14-P-150)

### PIN ASSIGNMENT



(TOP VIEW)

### IEC LOGIC SYMBOL



### TRUTH TABLE

A	B	Y
H	H	H
L	H	H
H	L	H
L	L	L

# TC74ACT32P/F/FN

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5 ~ 6.0	V
DC Input Voltage	$V_{IN}$	-0.5 ~ $V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5 ~ $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	±20	mA
Output Diode Current	$I_{OK}$	±50	mA
DC Output Current	$I_{OUT}$	±50	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	±100	mA
Power Dissipation	$P_D$	500(DIP)* / 180(SOP)	mW
Storage Temperature	$T_{stg}$	-65 ~ 150	°C
Lead Temperature 10sec	$T_L$	300	°C

\*500mW in the range of  $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$ . From  $T_a = 65^\circ\text{C}$  to  $85^\circ\text{C}$  a derating factor of  $-10\text{mW}/^\circ\text{C}$  shall be applied until 300mW.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	4.5 ~ 5.5	V
Input Voltage	$V_{IN}$	0 ~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0 ~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40 ~ 85	°C
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	$V_{IH}$		4.5 } 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	$V_{IL}$		4.5 } 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu\text{A}$ 4.5 $I_{OH} = -24\text{mA}$ 4.5 $I_{OH} = -75\text{mA}^*$ 5.5	4.4 3.94 -	4.5 -	- -	4.4 3.80 3.85	- -	V
Low-Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IL}$	$I_{OL} = 50 \mu\text{A}$ 4.5 $I_{OL} = 24\text{mA}$ 4.5 $I_{OL} = 75\text{mA}^*$ 5.5	- -	0.0 -	0.1 0.36 -	- -	0.1 0.44 1.65	V
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	-	-	4.0	-	40.0	μA
	$\Delta I_{CC}$	PER INPUT: $V_{IN} = 3.4\text{V}$ OTHER INPUT: $V_{CC}$ or GND	5.5	-	-	1.35	-	1.5	mA

\* This spec indicates the capability of driving 50Ω transmission lines.  
One output should be tested at a time for a 10ms maximum duration.

**AC ELECTRICAL CHARACTERISTICS(C<sub>L</sub>=50pF, R<sub>L</sub>=500Ω, Input t<sub>r</sub>=t<sub>f</sub>=3ns)**

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub>	T <sub>a</sub> =25°C			T <sub>a</sub> =-40 ~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t <sub>pLH</sub> t <sub>pHL</sub>		5.0±0.5	-	5.2	7.9	1.0	9.0	ns
Input Capacitance	C <sub>IN</sub>			-	5	10	-	10	pF
Power Dissipation Capacitance	C <sub>PD(1)</sub>			-	22	-	-	-	

Note (1) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(ops)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4(\text{per Gate})$$