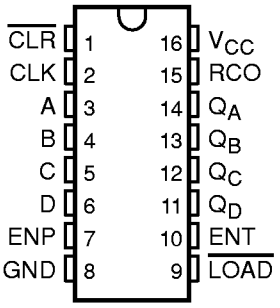
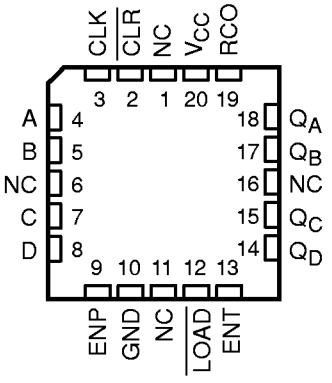
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

SN54LV163A . . . J OR W PACKAGE
SN74LV163A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV163A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'LV163A devices are 4-bit synchronous binary counters designed for 2-V to 5.5-V V_{CC} operation.

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'LV163A devices are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the 'LV163A devices is synchronous. A low level at the clear ($\overline{CLR}$) input sets all four of the flip-flop outputs low after the next low-to-high transition of CLK, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to $\overline{CLR}$ to synchronously clear the counter to 0000 (LLLL).

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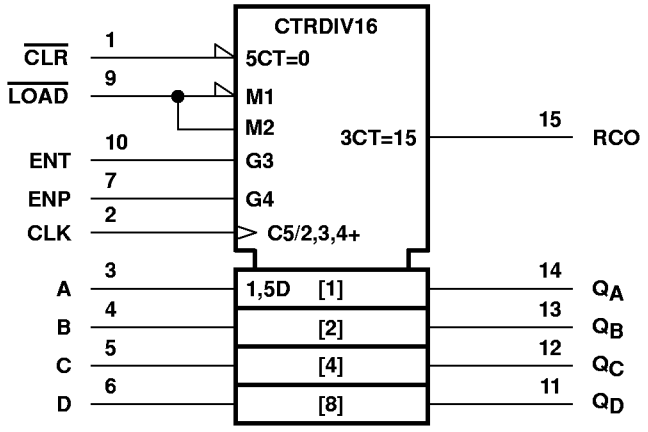
description (continued)

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP, ENT, and a ripple-carry output (RCO) are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The SN54LV163A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV163A is characterized for operation from –40°C to 85°C.

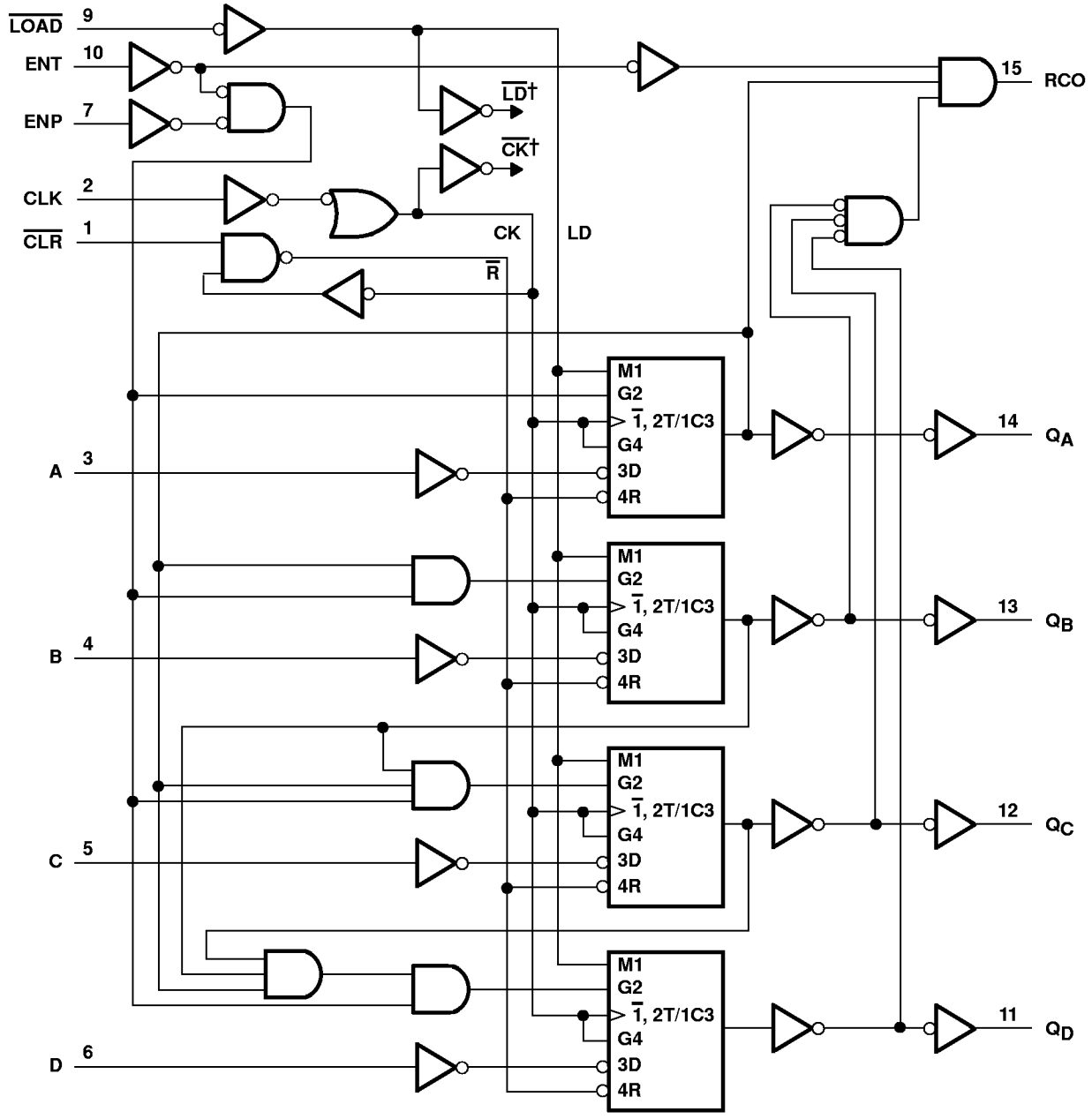
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

PRODUCT PREVIEW

logic diagram (positive logic)

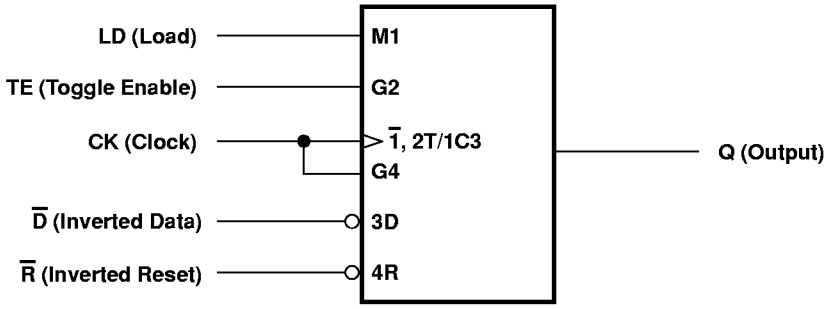


† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

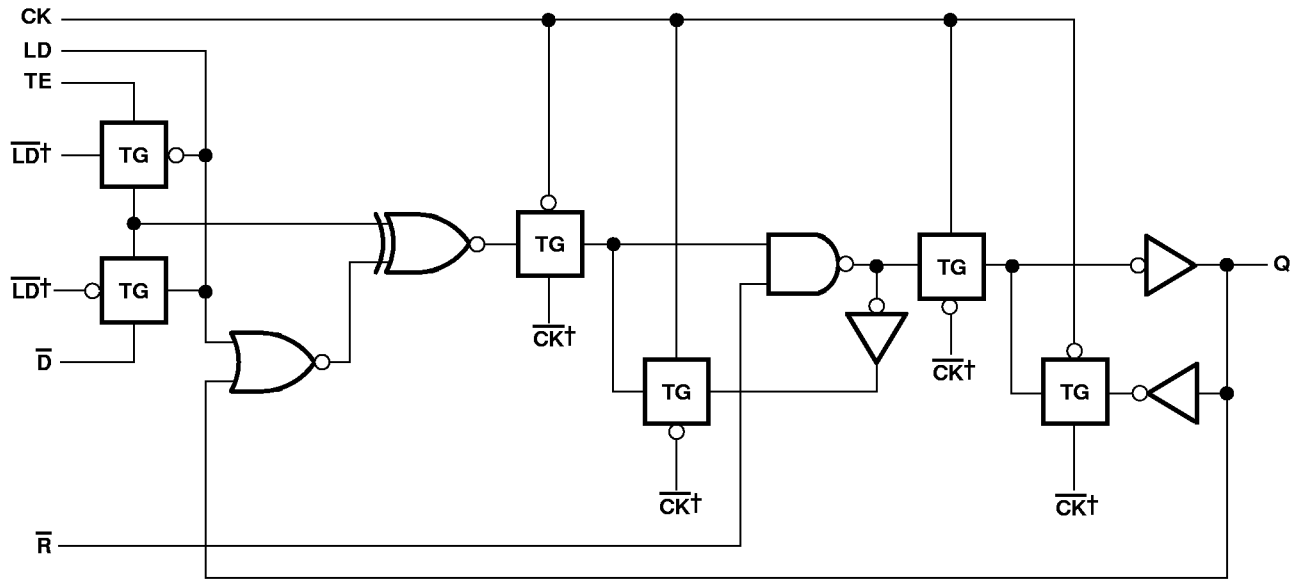
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

PRODUCT PREVIEW

logic symbol, each D/T flip-flop



logic diagram, each D/T flip-flop (positive logic)

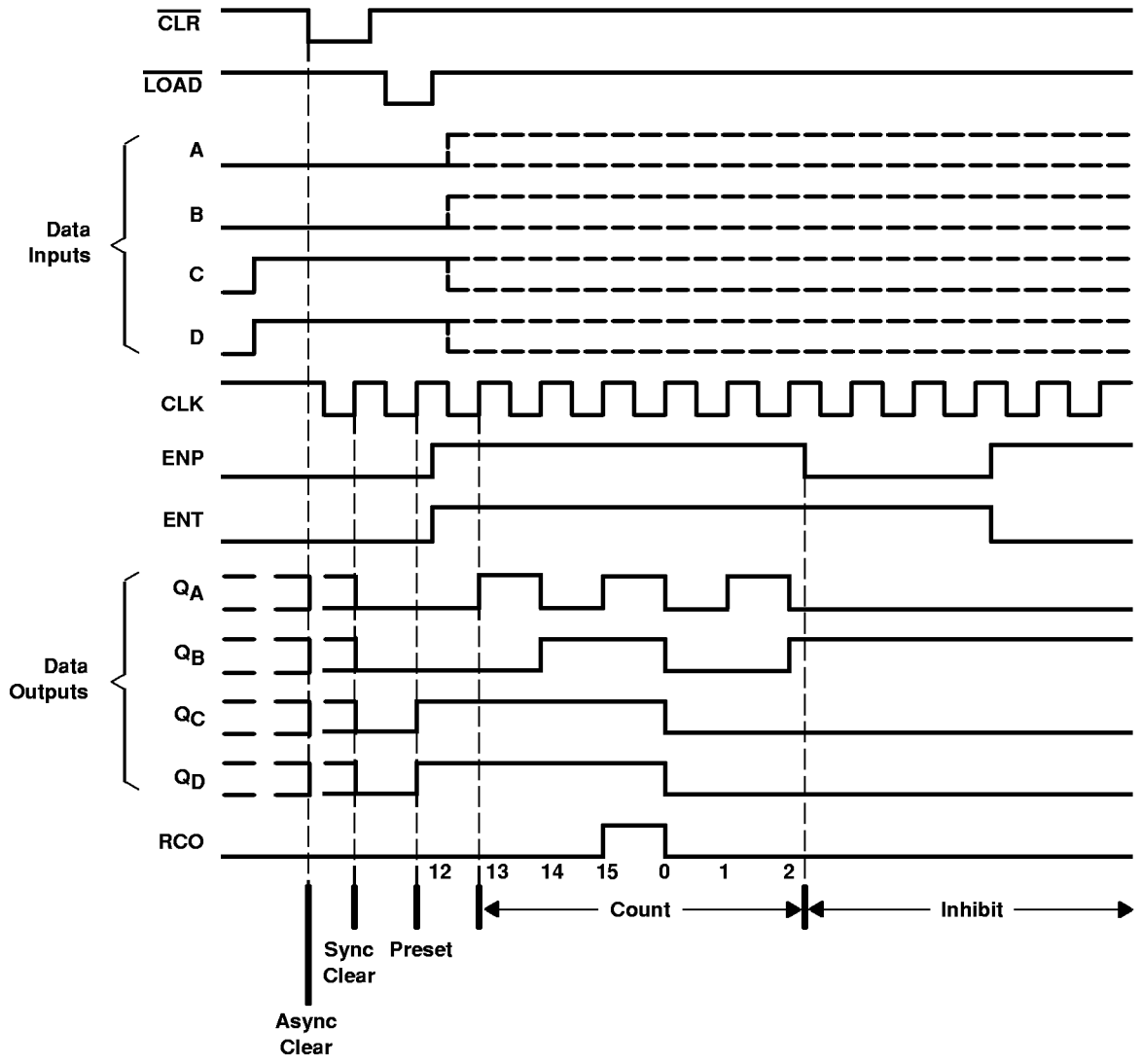


† The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagram of the overall device.

typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (synchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 113°C/W
DB package . . . . . 131°C/W
DGV package . . . . . 180°C/W
NS package . . . . . 111°C/W
PW package . . . . . 149°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

PRODUCT PREVIEW

recommended operating conditions (see Note 4)

			SN54LV163A		SN74LV163A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	µA
		V_{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V_{CC} = 3 V to 3.6 V		–6		–6	
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V_{CC} = 3 V to 3.6 V	0	100	0	100	
		V_{CC} = 4.5 V to 5.5 V	0	20	0	20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV163A			SN74LV163A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –50 μA	2 V to 5.5 V	V_{CC}–0.1			V_{CC}–0.1			V
	I_{OH} = –2 mA	2.3 V	2			2			
	I_{OH} = –6 mA	3 V	2.48			2.48			
	I_{OH} = –12 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4	
	I_{OL} = 6 mA	3 V			0.44			0.44	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	5.5 V			±1			±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	μA
I_{off}	V_I or V_O = 0 to 5.5 V	0 V			5			5	μA
C_i	V_I = V_{CC} or GND	3.3 V							pF
		5 V							

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV163A		SN74LV163A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low								ns
t_{su}	Setup time before CLK↑	$\overline{CLR}$							ns
		Data (A, B, C, and D)							
		ENP, ENT							
		$\overline{LOAD}$ low							
t_h	Hold time, all synchronous inputs after CLK↑								ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV163A		SN74LV163A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low								ns
t_{su}	Setup time before CLK↑	$\overline{CLR}$							ns
		Data (A, B, C, and D)							
		ENP, ENT							
		$\overline{LOAD}$ low							
t_h	Hold time, all synchronous inputs after CLK↑								ns

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV163A		SN74LV163A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low								ns
t_{su}	Setup time before CLK↑	$\overline{CLR}$							ns
		Data (A, B, C, and D)							
		ENP, ENT							
		$\overline{LOAD}$ low							
t_h	Hold time, all synchronous inputs after CLK↑								ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV163A		SN74LV163A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF*								MHz
			C_L = 50 pF								
t_{PLH}*	CLK	Q	C_L = 15 pF								ns
t_{PHL}*											
t_{PLH}*	CLK	RCO (count mode)									
t_{PHL}*											
t_{PLH}*	CLK	RCO (preset mode)									
t_{PHL}*											
t_{PLH}*	ENT	RCO									
t_{PHL}*											
t_{PLH}	CLK	Q	C_L = 50 pF								ns
t_{PHL}											
t_{PLH}	CLK	RCO (count mode)									
t_{PHL}											
t_{PLH}	CLK	RCO (preset mode)									
t_{PHL}											
t_{PLH}	ENT	RCO									
t_{PHL}											

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV163A		SN74LV163A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF*								MHz
			C_L = 50 pF								
t_{PLH}*	CLK	Q	C_L = 15 pF								ns
t_{PHL}*											
t_{PLH}*	CLK	RCO (count mode)									
t_{PHL}*											
t_{PLH}*	CLK	RCO (preset mode)									
t_{PHL}*											
t_{PLH}*	ENT	RCO									
t_{PHL}*											
t_{PLH}	CLK	Q	C_L = 50 pF								ns
t_{PHL}											
t_{PLH}	CLK	RCO (count mode)									
t_{PHL}											
t_{PLH}	CLK	RCO (preset mode)									
t_{PHL}											
t_{PLH}	ENT	RCO									
t_{PHL}											

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV163A		SN74LV163A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF*								MHz
			C_L = 50 pF								
t_{PLH}*	CLK	Q	C_L = 15 pF								ns
t_{PHL}*											
t_{PLH}*	CLK	RCO (count mode)									
t_{PHL}*											
t_{PLH}*	CLK	RCO (preset mode)									
t_{PHL}*											
t_{PLH}*	ENT	RCO									
t_{PHL}*											
t_{PLH}	CLK	Q	C_L = 50 pF								ns
t_{PHL}											
t_{PLH}	CLK	RCO (count mode)									
t_{PHL}											
t_{PLH}	CLK	RCO (preset mode)									
t_{PHL}											
t_{PLH}	ENT	RCO									
t_{PHL}											

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74LV163A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage				V
$V_{IL(D)}$	Low-level dynamic input voltage				V

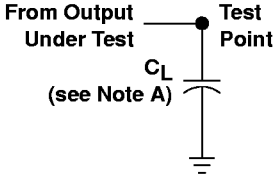
NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, T_A = 25°C

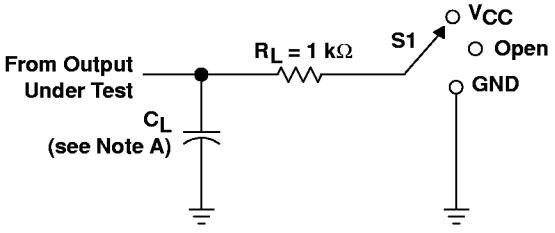
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V		pF
			5 V		

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

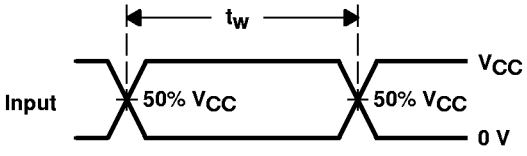


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

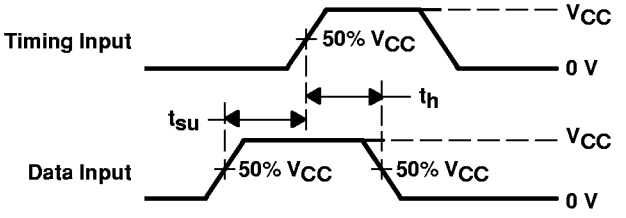


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

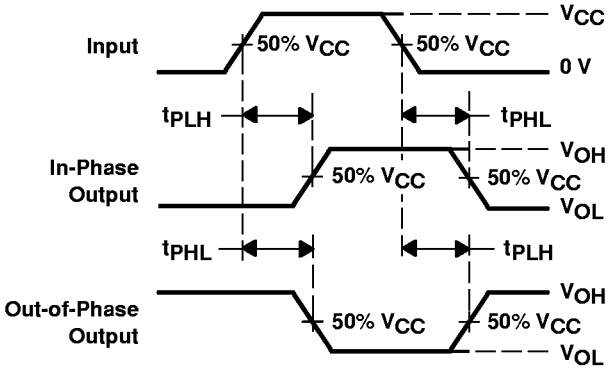
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



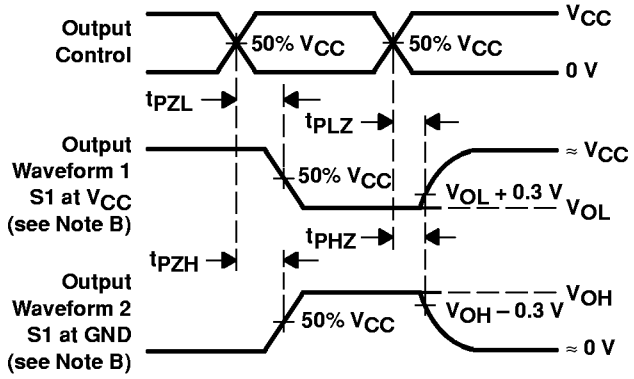
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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