54F/74F543

Octal Registered Transceiver

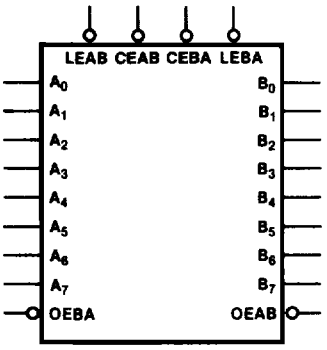
Description

The 'F543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 20 mA while the B outputs are rated for 64 mA.

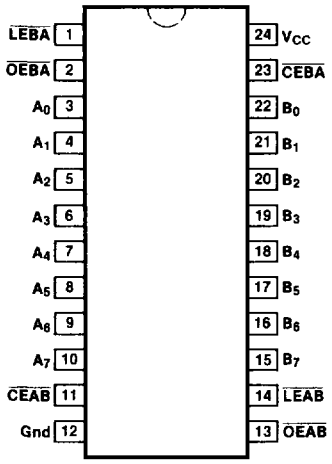
- **8-Bit Octal Transceiver**
- **Back-to-Back Registers for Storage**
- **Separate Controls for Data Flow in Each Direction**
- **B Outputs Sink 64 mA**
- **300 mil Slim Package**

Ordering Code: See Section 5

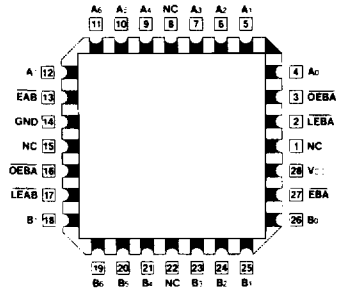
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)	0.5/0.375
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)	0.5/0.375
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)	0.5/0.75
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)	0.5/0.75
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)	0.5/0.375
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)	0.5/0.375
A_0-A_7	A-to-B Data Inputs or	1.75/0.406
	B-to-A 3-State Outputs	25/12
B_0-B_7	B-to-A Data Inputs or	1.75/0.406
	A-to-B 3-State Outputs	75/40 (30)

Functional Description

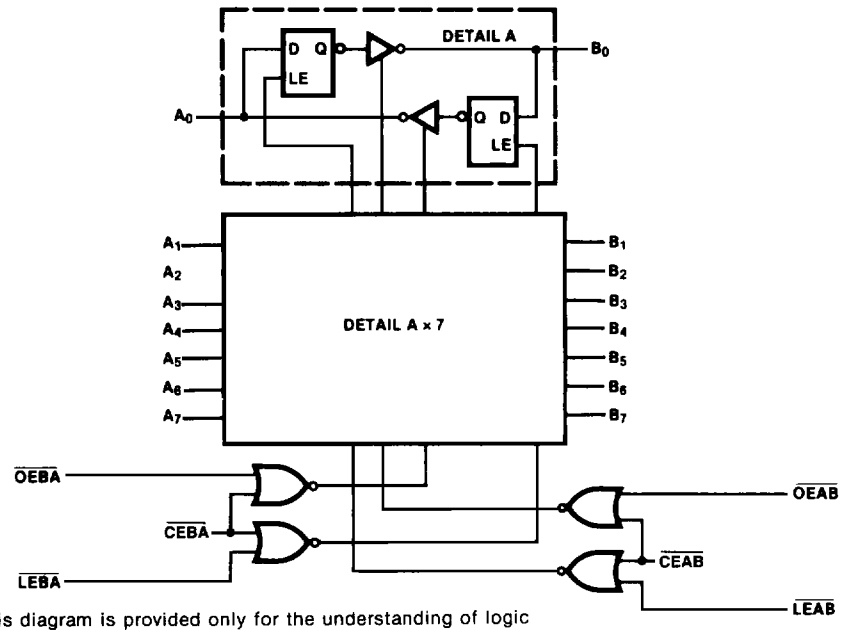
The 'F543 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0-A_7 or take data from B_0-B_7, as indicated in the Data I/O Control Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEAB}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{EAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B_0-B_7
H	X	X	Storing	High Z
X	H		Storing	
X		H		High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

* Before $\overline{LEAB}$ LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH} I_{CCL} I_{CCZ}	Power Supply Current		67 83 83	100 125 125	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay, Transparent Mode A_n to B_n or B_n to A_n	3.0 3.0	5.5 5.0	7.5 6.5			3.0 3.0	8.5 7.5	ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A_n	4.5 4.5	8.5 8.5	11.0 11.0			4.5 4.5	12.5 12.5	ns	3-1 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAB}$ to B_n	4.5 4.5	8.5 8.5	11.0 11.0			4.5 4.5	12.5 12.5	ns	3-1 3-8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	3.0 4.0	7.0 7.5	9.0 10.5			3.0 4.0	10.0 12.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	2.5 2.5	6.0 5.5	8.0 7.5			2.5 2.5	9.0 8.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_s(H) t_s(L)	Setup Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	3.0 3.0					3.5 3.5		ns	3-14
t_h(H) t_h(L)	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	3.0 3.0					3.5 3.5			
t_w(L)	Latch Enable, B to A Pulse Width, LOW	8.0					9.0		ns	3-7