HARRIS Semiconductor

CD74LPT16646

December 1996

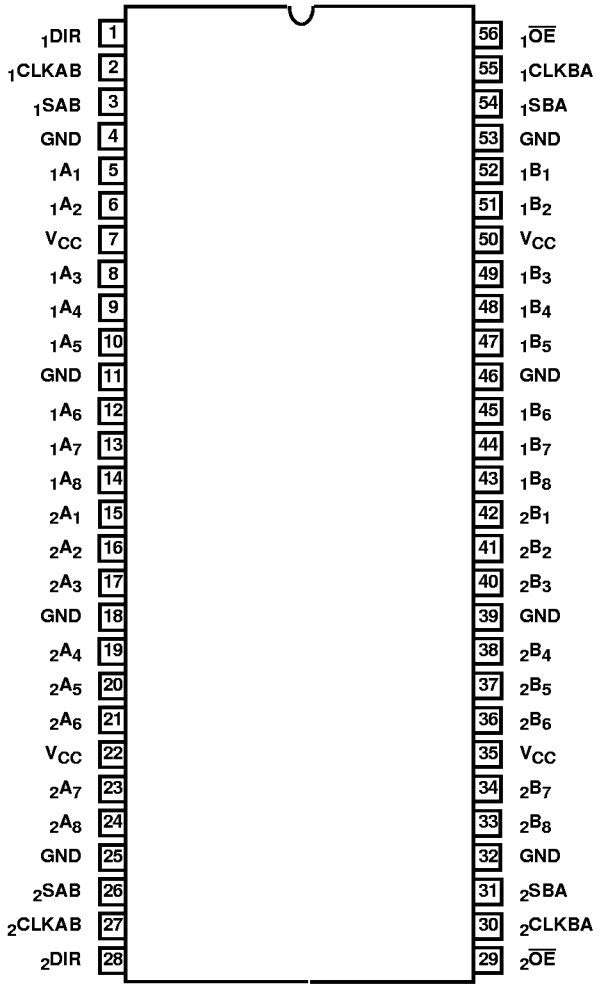
Fast CMOS 3.3V 16-Bit Registered Transceiver

Features

- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
- Input Can Be 3V or 5V
- Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability
  - Balanced Drives (24mA Sink and Source)
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise

Pinout

CD74LPT16646 (SSOP, TSSOP)
TOP VIEW



Description

Harris Semiconductor's CD74LPT16646 is produced in an advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The CD74LPT16646 is a 16-bit registered transceiver organized as two independent 8-bit bus transceivers designed with three-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Each 8-bit transceiver utilizes the enable control ($_X\overline{OE}$) and direction pins ($_X$DIR) to control the transceiver functions. The Select ($_X$SAB and $_X$SBA) control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The CD74LPT16646 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Ordering Information

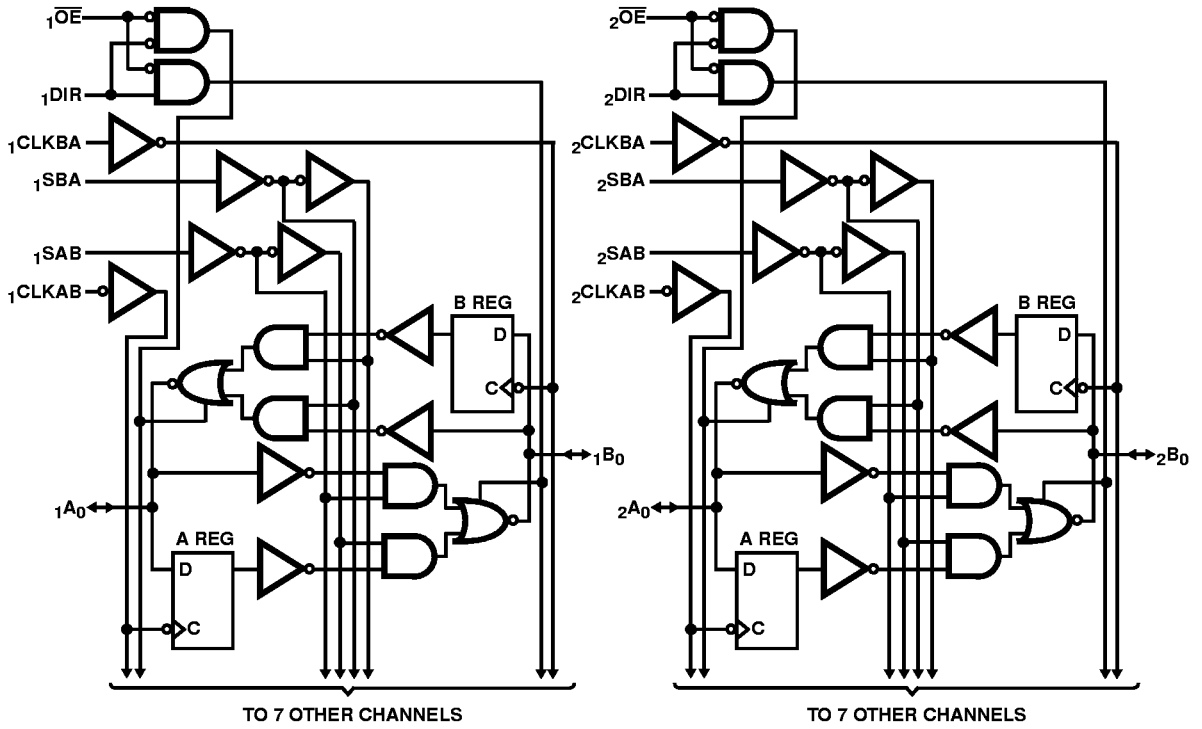
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CD74LPT16646AMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16646ASM	-40 to 85	56 Ld SSOP	M56.300-P
CD74LPT16646MT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16646SM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the varient in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4210.1**

Functional Block Diagram



TRUTH TABLE (NOTE 2)

FUNCTION	INPUTS						(Note 1) DATA I/O	
	$_X\overline{OE}$	$_X$DIR	$_X$CLKAB	$_X$CLKBA	$_X$SAB	$_X$SBA	$_XA_X$	$_XB_X$
Isolation	H	X	H or L	H or L	X	X	Input	Input
Store A and B Data	H	X	↑	↑	X	X		
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	L	H	X	X	L	X	Input	Output
Stored A Data to B Bus	L	H	H or L	X	H	X		

NOTES:

1. The data output functions may be enabled or disabled by various signals at the $_X\overline{OE}$ or $_X$DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH transition

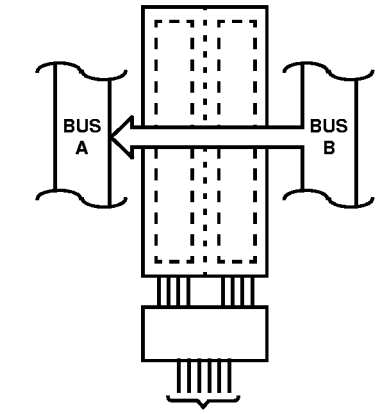


FIGURE 1. REAL-TIME TRANSFER BUS B TO A

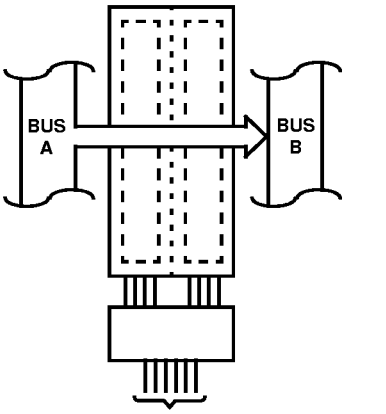


FIGURE 2. REAL-TIME TRANSFER BUS A TO B

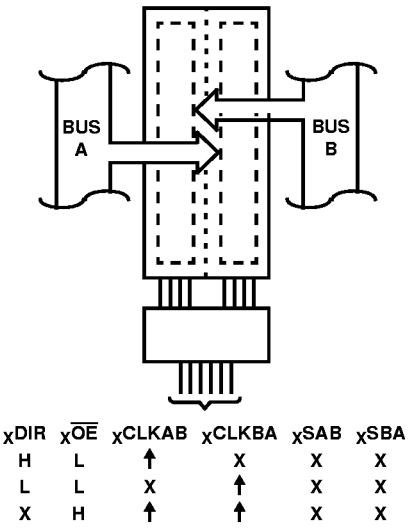


FIGURE 3. STORAGE FROM A AND/OR B

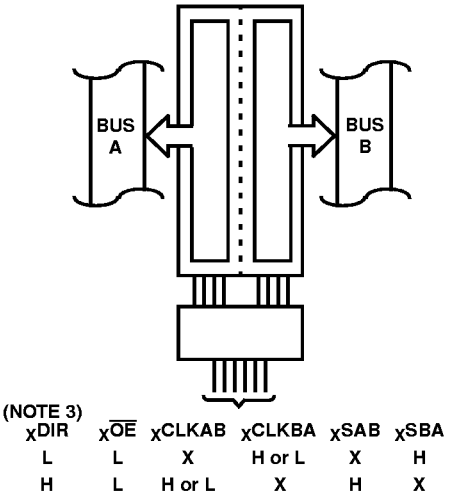


FIGURE 4. TRANSFER STORES DATA TO A AND/OR B

NOTE:

3. Cannot transfer data to A bus and B bus simultaneously.

Pin Descriptions

PIN NAME	DESCRIPTION
$_X\overline{OE}$, $_X$DIR	Output Enable Inputs (Active LOW)
$_X$CLKAB, $_X$CLKBA	Clock Pulse Inputs
$_X$SAB, $_X$SBA	Output Data Source Select Inputs
$_XA_X$	Data Register A Inputs Data Register B Outputs
$_XB_X$	Data Register B Inputs Data Register A Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . $-40^{o}C$ to $85^{o}C$
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} ($^{o}C/W$)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^{o}C$ to $85^{o}C$, $V_{CC} = 2.7V$ to $3.6V$							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	$V_{IN} = 5.5V$	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	$V_{OUT} = 5.5V$	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	$V_{CC} = Min$, $I_{IN} = -18mA$		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	$V_{CC} = 3.3V$, $V_{IN} = V_{IH}$ or V_{IL}, $V_O = 1.5V$ (Note 7)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	$V_{CC} = 3.3V$, $V_{IN} = V_{IH}$ or V_{IL}, $V_O = 1.5V$ (Note 7)		50	90	200	mA
Output HIGH Voltage	V_{OH}	$V_{CC} = Min$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -0.1mA$	V_{CC} - 0.2	-	-	V
			$I_{OH} = -3mA$	2.4	3.0	-	V
		$V_{CC} = 3.0V$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -8mA$	2.4 (Note 9)	3.0	-	V
			$I_{OH} = -24mA$	2.0	-	-	V
Output LOW Voltage	V_{OL}	$V_{CC} = Min$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 0.1mA$	-	-	0.2	V
			$I_{OL} = 16mA$	-	0.2	0.4	V
			$I_{OL} = 24mA$	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
Short Circuit Current (Note 8)	I_{OS}	V_{CC} = Max (Note 7), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC}$ - 0.6V (Note 11)	-	2.0	30	µA
Dynamic Power Supply Current (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 14)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_I = 2.5MHz, 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 13)	mA

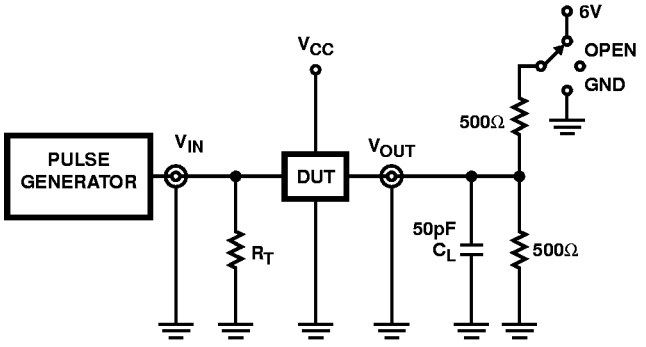
Switching Specifications Over Operating Range (Note 15)

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	CD74LPT16646		CD74LPT16646A		UNITS
			(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	
Propagation Delay Bus to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	ns
Output Enable Time $_X$DIR or $_X\overline{OE}$ to Bus	t_{PZH}, t_{PZL}		2.0	14.0	2.0	9.8	ns
Output Disable Time (Note 18) $_X$DIR or $_X\overline{OE}$ to Bus	t_{PHZ}, t_{PLZ}		2.0	9.0	2.0	6.3	ns
Propagation Delay Clock to Bus	t_{PLH}, t_{PHL}		2.0	9.0	2.0	6.3	ns
Propagation Delay $_X$SBA or $_X$SAB to Bus	t_{PLH}, t_{PHL}		2.0	11.0	2.0	7.7	ns
Setup Time HIGH or LOW, Bus to Clock	t_{SU}		4.0	-	2.0	-	ns
Hold Time HIGH or LOW, Bus to Clock	t_H		2.0	-	1.5	-	ns
Clock Pulse Width HIGH or LOW (Note 18)	t_W		6.0	-	5.0	-	ns
Output Skew (Note 19)	$t_{SK(O)}$		-	0.5	-	0.5	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. This parameter is guaranteed but not tested.
9. $V_{OH} = V_{CC}$ - 0.6V at rated current.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input; all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
15. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
16. See test circuit and wave forms.
17. Minimum limits are guaranteed but not tested on Propagation Delays.
18. This parameter is guaranteed but not production tested.
19. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

20. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 5. TEST CIRCUIT

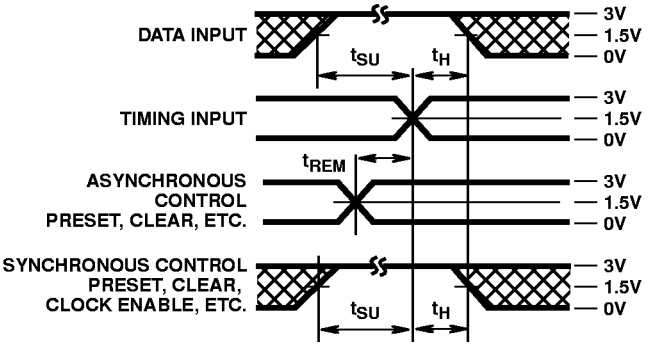


FIGURE 6. SETUP, HOLD, AND RELEASE TIMING

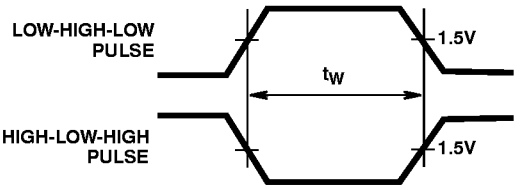


FIGURE 7. PULSE WIDTH

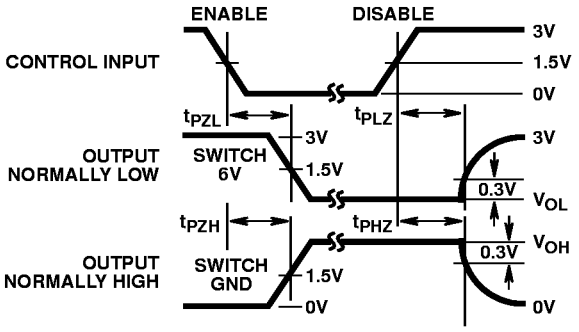


FIGURE 8. ENABLE AND DISABLE TIMING

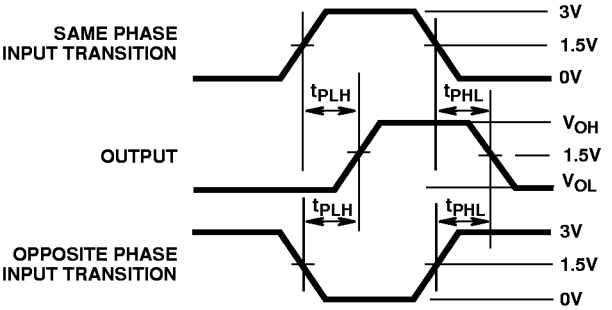


FIGURE 9. PROPAGATION DELAY