TC74AC74P/F/FN

DUAL D-TYPE FLIP FLOP PRESET AND CLEAR

The TC74AC74 is an advanced high speed CMOS D-FLIP FLOP fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

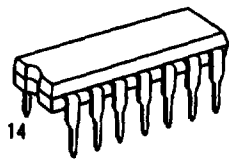
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

$\overline{CLR}$ and $\overline{PR}$ are independent of the CK and are accomplished by setting the appropriate input low.

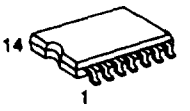
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

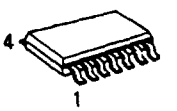
FEATURES:

- High Speed ..... f_{max}=200MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 74



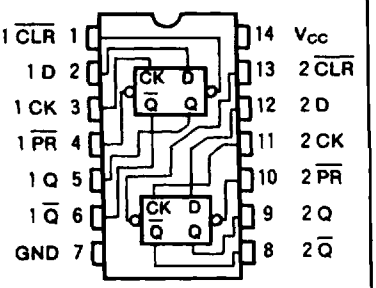
P(DIP14-P-300)





F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



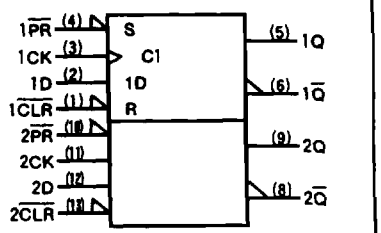
(TOP VIEW)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	↓	L	H	—
H	H	H	↓	H	L	—
H	H	X	↑	Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

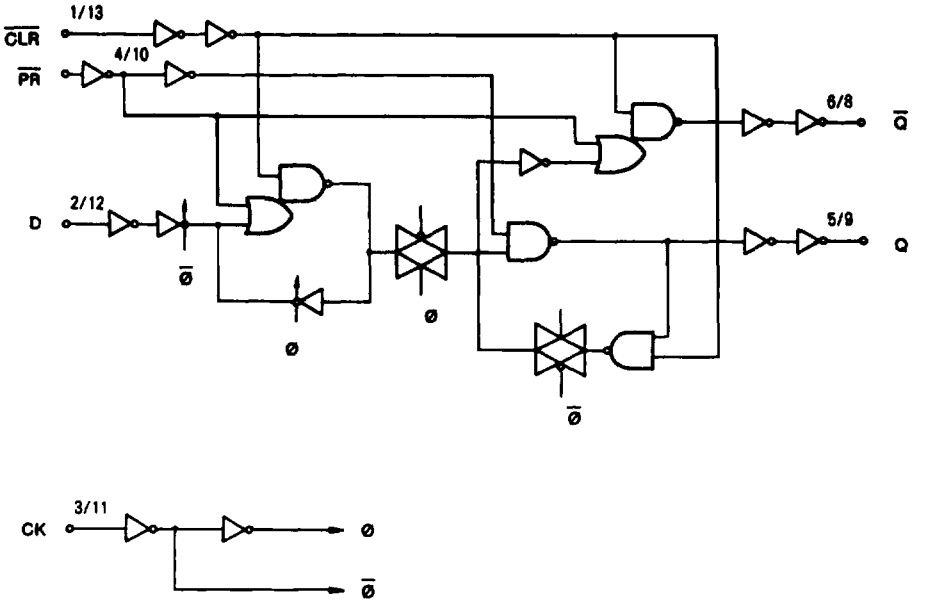
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40∼85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$		3.3±0.3	−	7.0	7.0	ns
	$t_{W(H)}$		5.0±0.5	−	5.0	5.0	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{W(L)}$		3.3±0.3	−	7.0	7.0	
			5.0±0.5	−	5.0	5.0	
Minimum Set-up Time	t_s		3.3±0.3	−	6.0	6.0	
			5.0±0.5	−	3.5	3.5	
Minimum Hold Time	t_h		3.3±0.3	−	1.0	1.0	
			5.0±0.5	−	1.0	1.0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		3.3±0.3	−	4.0	4.0	
			5.0±0.5	−	2.0	2.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	8.2	13.9	1.0	16.0	ns
	t_{pHL}		5.0±0.5	−	6.1	8.7	1.0	10.0	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$−Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	8.0	13.1	1.0	15.0	
	t_{pHL}		5.0±0.5	−	5.7	8.2	1.0	9.4	
Maximum Clock Frequency	f_{MAX}		3.3±0.3	60	120	−	60	−	MHz
			5.0±0.5	100	160	−	100	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	77	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/2 \text{ (per F/F)}$$