

Fast CMOS 16-Bit Registered Transceivers

Product Features:

Common Features:

- PI74FCT16652T and PI74FCT162652T are high-speed, low power devices with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A56)
 - 56-pin 300 mil wide plastic SSOP (V56)

PI74FCT16652T Features:

- High output drive: $I_{OH} = -32\text{ mA}$; $I_{OL} = 64\text{ mA}$
- Power off disable outputs permit “live insertion”
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162652T Features:

- Balanced output drivers: $\pm 24\text{ mA}$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Product Description:

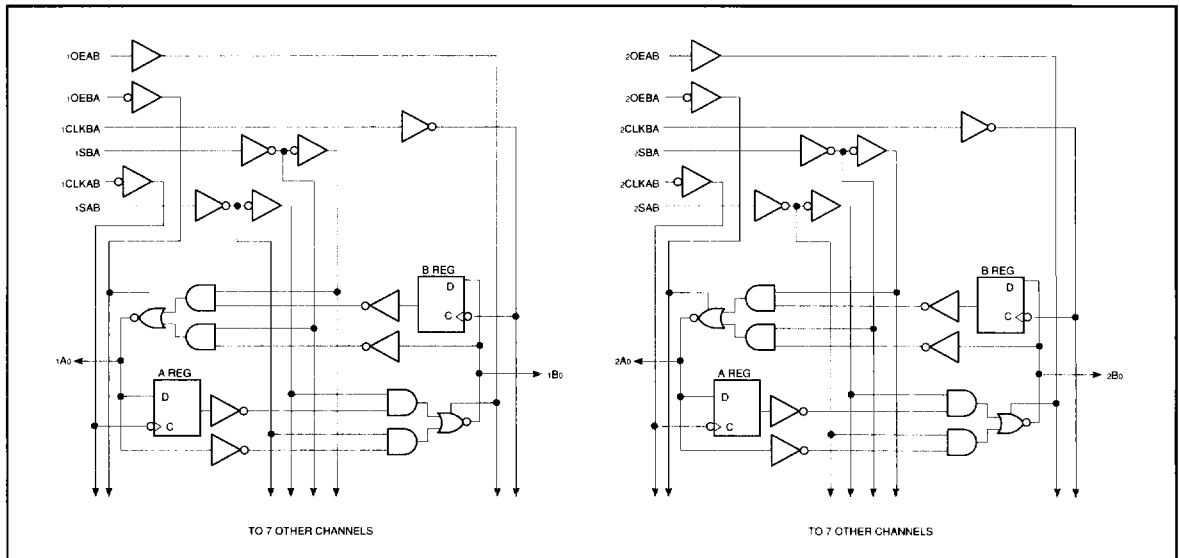
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT16652T and PI74FCT162652T are 16-bit registered transceivers organized as two independent 8-bit bus transceivers designed with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Each 8-bit transceiver utilizes the enable controls (\overline{xOEAB} and \overline{xOEBA}) to control the transceiver functions. The Select (\overline{xSAB} and \overline{xSBA}) control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The PI74FCT16652T output buffers are designed with a Power-Off disable allowing “live insertion” of boards when used as backplane drivers.

The PI74FCT162652T has $\pm 24\text{ mA}$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Logic Block Diagram

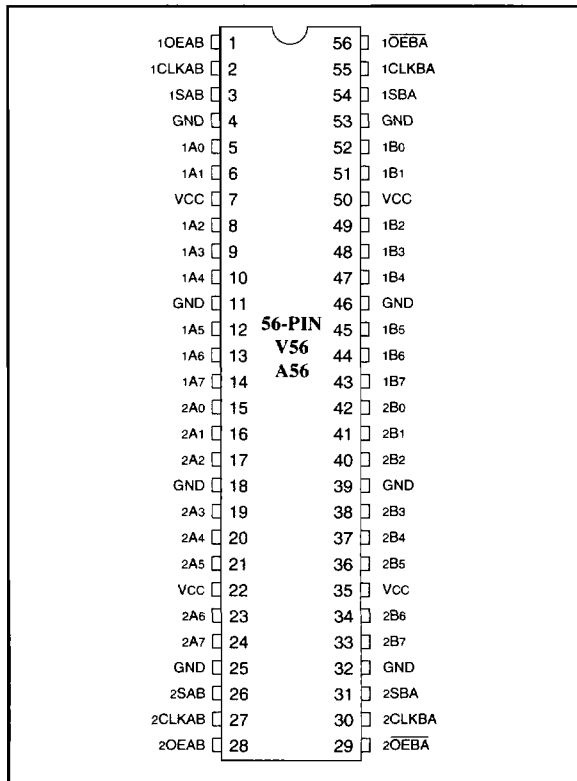


Truth Table

Function/Operation	Inputs						DATA I/O ⁽²⁾	
	xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx
Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B Data	L	H	↑	↑	X	X		
Store A, Hold B	X	H	↑	H or L	X	X	Input	Unspecified ⁽¹⁾
Store A in Both Registers	H	H	↑	↑	X ⁽²⁾	X	Input	Output
Hold A, Store B	L	X	H or L	↑	X	X	Unspecified ⁽¹⁾	Input
Store B in Both Registers	L	L	↑	↑	X	X ⁽²⁾	Output	Input
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	H	H	X	X	L	X	Input	Output
Stored A Data to B Bus	H	H	H or L	X	H	X		
Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

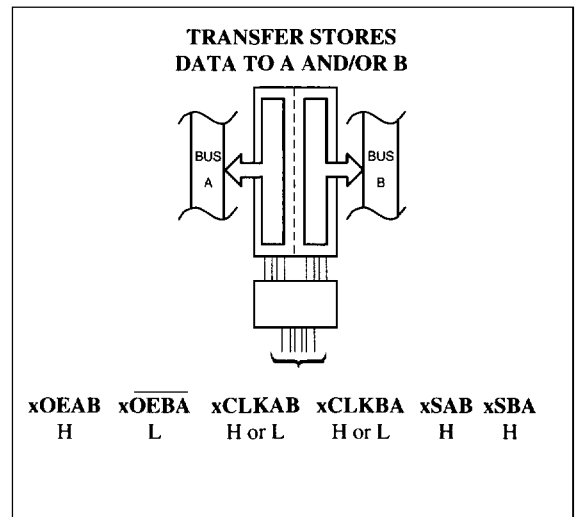
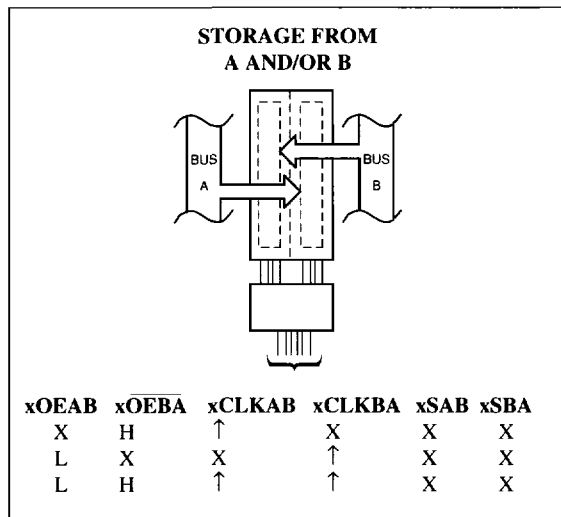
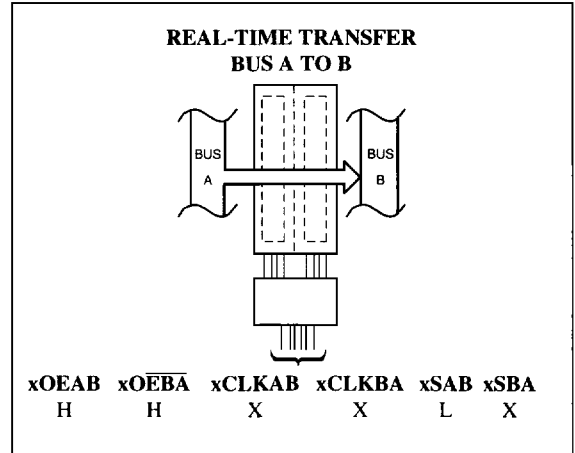
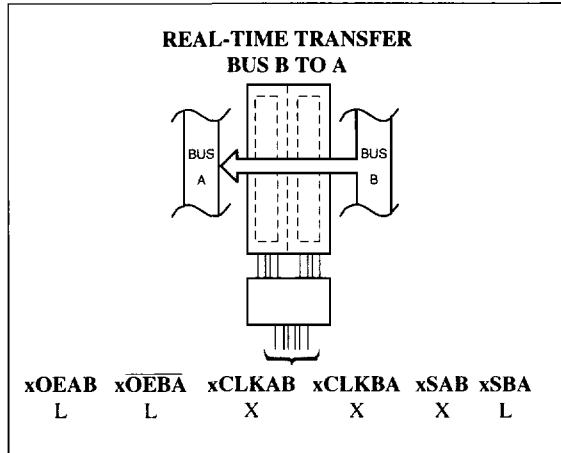
- The data output functions may be enabled or disabled by various signals at the xOEAB or xOEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
- Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.
H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = LOW-to-HIGH transition

Product Pin Configuration



Product Pin Description

Pin Name	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
xOEAB, xOEBA	Output Enable Inputs
GND	Ground
Vcc	Power



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

 Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	V _{CC} = Max., V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	V _{CC} = Max., V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND	-80	-140	-200	mA
I _O	Output Drive Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = 2.5V	-50		-180	mA
V _H	Input Hysteresis			100		mV

PI74FCT16652T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.0 mA	2.5	3.5		V
			I _{OH} = -15.0 mA	2.4	3.5		
			I _{OH} = -32.0 mA	2.0	3.0		
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}		0.2	0.55	V	
I _{OFF}	Power Down Disable	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V	—	—	±100	μA	

PI74FCT162652T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}		3.3		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}		0.3	0.55	V
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	60	115	150	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	-60	-115	-150	mA

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	500	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open xOEAB = xOEBA = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		75	120	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz (xCLKBA) 50% Duty Cycle xOEAB = xOEBA = GND One Bit Toggling fi = 5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.8	1.7 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		1.3	3.2 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz (xCLKBA) 50% Duty Cycle xOEAB = xOEBA = GND 16 Bits Toggling fi = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		3.8	6.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		8.3	22.0 ⁽⁵⁾	

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

$$6. I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16652 Switching Characteristics over Operating Range

Parameters	Description	Conditions ¹⁾	16652T		16652AT		16652CT		16652DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	C _L = 50 pF R _L = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.4	ns
t _{PZH} t _{PZL}	Output Enable Time xOEAB or xOEBA to Bus		2.0	14.0	2.0	9.8	1.5	7.8	1.5	5.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time ³⁾ xOEAB or xOEBA to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	4.3	ns
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	4.4	ns
t _{PLH} t _{PHL}	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	7.7	1.5	6.2	1.5	5.0	ns
t _{SU}	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	ns
t _H	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.0	—	ns
t _W	Clock Pulse Width HIGH or LOW ³⁾		6.0	—	5.0	—	5.0	—	3.0	—	ns
t _{SK(O)}	Output Skew ⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

PI74FCT162652 Switching Characteristics over Operating Range

Parameters	Description	Conditions ¹⁾	162652T		162652AT		162652CT		162652DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	C _L = 50 pF R _L = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.4	ns
t _{PZH} t _{PZL}	Output Enable Time xOEAB or xOEBA to Bus		2.0	14.0	2.0	9.8	1.5	7.8	1.5	5.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time ³⁾ xOEAB or xOEBA to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	4.3	ns
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	4.4	ns
t _{PLH} t _{PHL}	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	7.7	1.5	6.2	1.5	5.0	ns
t _{SU}	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	ns
t _H	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.0	—	ns
t _W	Clock Pulse Width HIGH or LOW ³⁾		6.0	—	5.0	—	5.0	—	3.0	—	ns
t _{SK(O)}	Output Skew ⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This limit is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.