SGS-THOMSON MICROELECTRONICS

M54/74HCT651
M54/74HCT652

HCT651 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE, INV.)
HCT652 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE)

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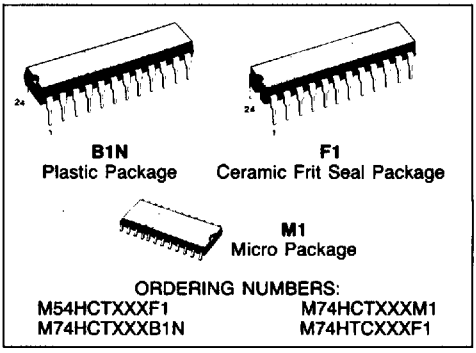
- LOW POWER DISSIPATION
  I_{CC} = 4μA (MAX.) at T_A = 25°C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LST651/652



B1N
Plastic Package

F1
Ceramic Frit Seal Package

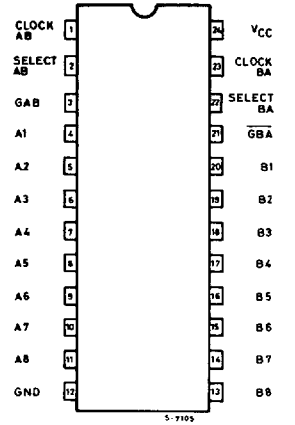
M1
Micro Package

ORDERING NUMBERS:
M54HCTXXXF1 M74HCTXXXM1
M74HCTXXXB1N M74HTCXXXF1

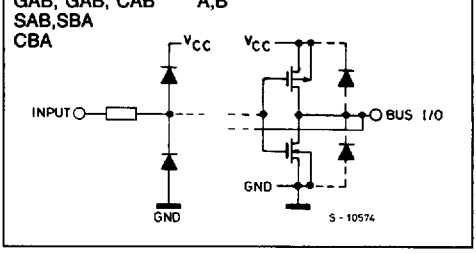
DESCRIPTION

The M54/74HCT651-652 are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTER fabricated in silicon gate C²MOS technology.
They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices consists of bus transceiver circuits, D-type flip-flop, and control circuitry arranged for multiplex transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{GBA}$ are provided to control the transceiver functions. Select AB and select BA control pins are provided to select the real-time or stored data function. Data on the A or B DATA bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CLOCK AB or CLOCK BA) regardless of the select or enable control pins.
When select AB and select BA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{GBA}$. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.
All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuit has totally compatible, input and output characteristic, with standard 54/74 LSTTL logic families.
M54HCT/74HCT devices are designed to interface directly with HSC²MOS components. These devices are also plug in relacements for LSTTL device giving a reduction in power consumption.

PIN CONNECTIONS (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



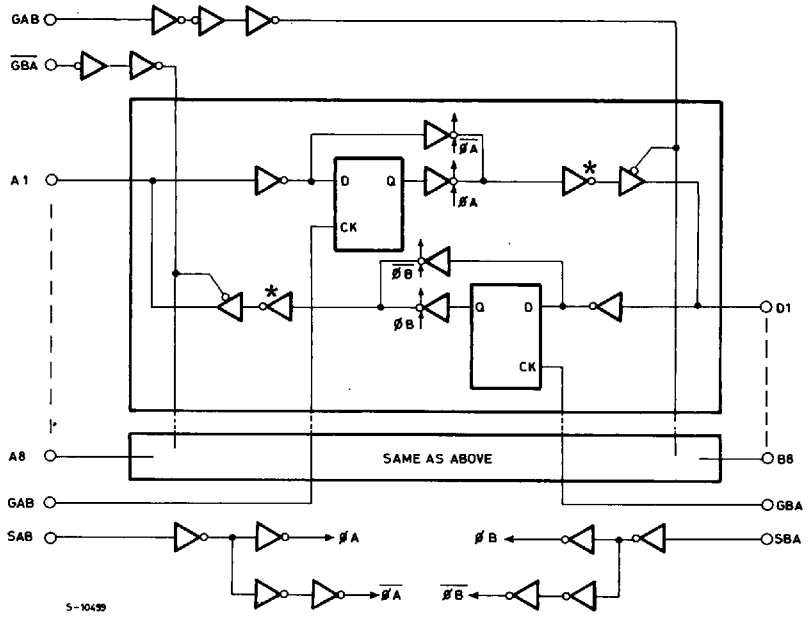
TRUTH TABLE

M54/74HCT652 (The truth table for M54/74HCT651 is the same as this, but with the outputs inverted)

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	FUNCTION
L	H					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		↓	↓	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	L					OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
		X*	↓	X	L	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are dispayed at the A bus.
		X*	↓	X	H	H L	H L	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.
H	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
		↓	X*	L	X	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↓	X*	H	X	L H	H	The data at the A bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus.
H	L					OUTPUTS	OUTPUTS	Both the A bus and the B bus are outputs.
		X	X	H	H	Qn	Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively.
		↓	↓	H	H	Qn	Qn	The output at the A bus are displayed at the B bus, the output at the B bus are displayed at the A bus respec.

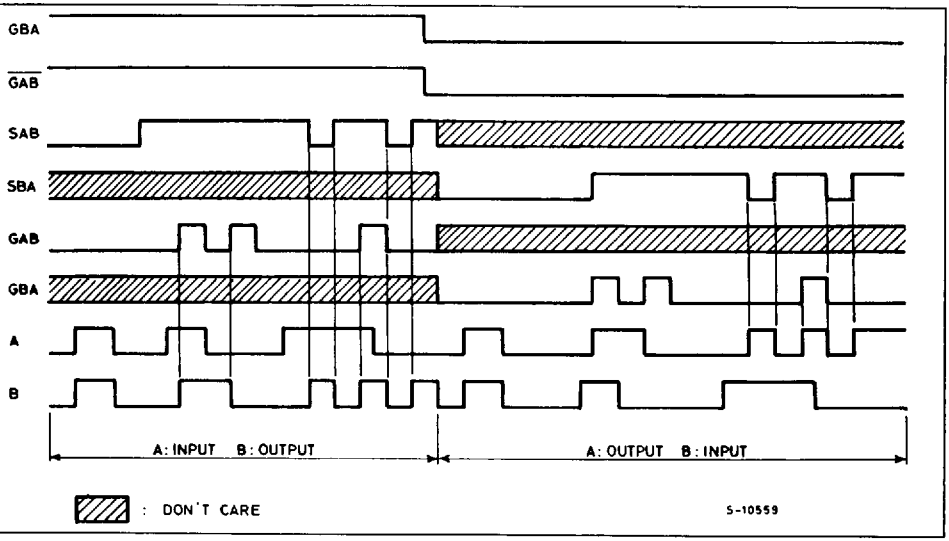
X : DON'T CARE.
Z : HIGH IMPEDANCE.
Qn : THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS.
* : THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO TRANSITION OF THE CLOCK INPUTS.

LOGIC DIAGRAM (HC651) S G S-THOMSON



NOTE: IN CASE OF M54/74HCT652 OUTPUT INVERTER MARKED * AT A BUS AND B BUS ARE ELIMINTATED

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

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Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		4.5 to 5.5	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 − 55 to 125	°C
t_r, t_f	Input Rise and Fall Time		0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0	—	—	2.0	—	2.0	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage	4.5	V_{IN}	I_{OH}								
			V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	V
				−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	

DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	4.5	V_{IN}	I_{OL}								
			V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
				6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current*	5.5	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-State Output Off-State Current	5.5	$V_I = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10.0	μA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA
I_C			Per input: $V_{IN} = 2.4V$ or 0.5V Other input: V_{CC} or GND		—	—	2.0	—	2.9	—	3.0	mA

*: Applicable only to GAB, $\overline{GBA}$, CAB, CBA, SAB, SBA input

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	7	12	—	15	—	18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (BUS-BUS)	4.5		—	20	31	—	39	—	47	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-BUS)	4.5		—	30	47	—	58	—	71	ns
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT-BUS)	4.5		—	31	48	—	60	—	72	ns
$t_{W(H)}$ $t_{W(L)}$	Minimum Clock Pulse Width	4.5		—	11	20	—	25	—	30	ns

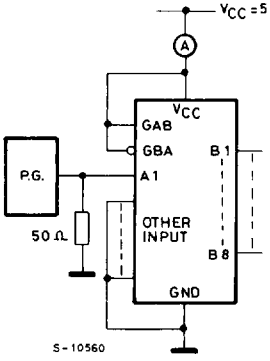
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_s	Minimum Data Set-up Time	4.5		—	4	10	—	13	—	15	ns
t_h	Minimum Data Hold Time	4.5		—	—	5	—	5	—	5	ns
t_{PZL} t_{PZH}	3-State Output Enable Time ($\overline{GBA}$ - BUS)	4.5	$R_L = 1k\Omega$	—	21	30	—	38	—	45	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time (GBA - BUS)	4.5	$R_L = 1k\Omega$	—	26	38	—	48	—	57	ns
t_{PZL} t_{PZH}	3-State Output Enable Time (GAB - BUS)	4.5	$R_L = 1k\Omega$	—	25	36	—	45	—	54	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time (GAB - BUS)	4.5	$R_L = 1k\Omega$	—	25	36	—	45	—	54	ns
C_{IN}	Input Capacitance*			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance		BUS I/O	—	13	—	—	—	—	—	
C_{PD} (1)	Power Dissipation Capacitance		HCT651	—	52	—	—	—	—	—	
			HCT652	—	52	—	—	—	—	—	

* Applicable only to GAB, $\overline{GBA}$, CAB, CBA, SAB, SBA input.

Note (1) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained by equation hereunder.
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TEST CIRCUIT I_{CC} (Opr.)



INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SWITCHING CHARACTERISTICS TEST WAVEFORM

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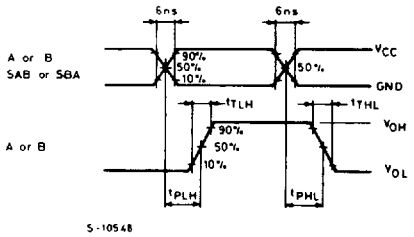
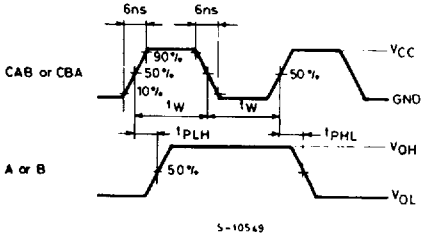
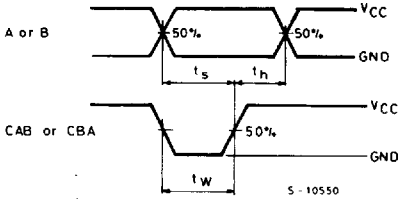
WAVEFORM 1



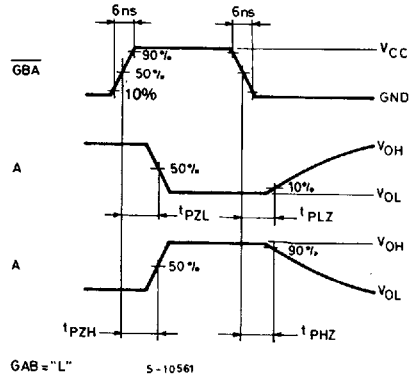
WAVEFORM 2



WAVEFORM 3



WAVEFORM 4



WAVEFORM 5