MOTOROLA

SN54/74LS107A

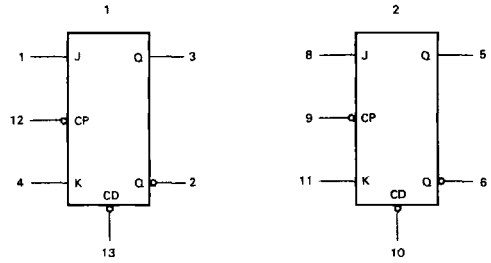
DESCRIPTION — The SN54LS/74LS107A is a Dual JK Flip-Flop with individual J, K, Direct Clear and Clock Pulse inputs. Output changes are initiated by the HIGH-to-LOW transition of the clock. A LOW signal on CD input overrides the other inputs and makes the Q output LOW.

The SN54LS/74LS107A is the same as the SN54LS/74LS73A but has corner power pins.

DUAL JK FLIP-FLOP

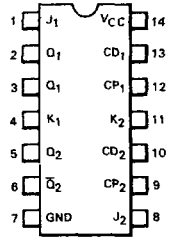
LOW POWER SCHOTTKY

LOGIC SYMBOL



V_{CC} = 14
GND = 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current	J, K Clear Clock			20 60 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
		J, K Clear Clock			0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current	J, K Clear and Clock			−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				6.0	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
f_{MAX}	Maximum Clock Frequency	30	45		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH}	Propagation Delay,		15	20	ns	
t_{PHL}	Clock to Output		15	20	ns	

AC SETUP REQUIREMENTS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_W	Clock Pulse Width	20			ns	V_{CC} = 5.0 V
t_W	Clear Pulse Width	25			ns	
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	