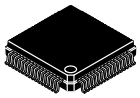
Product Preview

Low-Voltage 1:22 Differential PECL/HSTL Clock Driver

MC100EP223

LOW–VOLTAGE 1:22 DIFFERENTIAL PECL/HSTL CLOCK DRIVER



FA SUFFIX
64–LEAD TQFP PACKAGE
CASE 840F–02

The MC100EP223 is a low skew 1–to–22 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The selected signal is fanned out to 22 identical differential outputs.

- 200ps Part–to–Part Skew
- 50ps Output–to–Output Skew
- Differential Design
- Open Emitter HSTL Compatible Outputs
- 3.3V V_{CC}
- Both PECL and HSTL Inputs
- 75kΩ Input Pulldown Resistors

The EP223 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate–to–gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

The EP223 HSTL outputs are not realized in the conventional manner. To minimize part–to–part and output–to–output skew, the HSTL compatible output levels are generated with an open emitter architecture. The outputs are pulled down with 50Ω to ground, rather than the typical 50Ω to V_{DDQ} pullup of a “standard” HSTL output. Because the HSTL outputs are pulled to ground, the EP223 does not utilize the V_{DDQ} supply of the HSTL standard. The output levels are derived from V_{CC}.

In the case of an asynchronous control, there is a chance of generating a ‘runt’ clock pulse when the device is enabled/disabled. To avoid this, the output enable (OE) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all 22 differential pairs will be used and therefore terminated. In the case where fewer than 22 pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

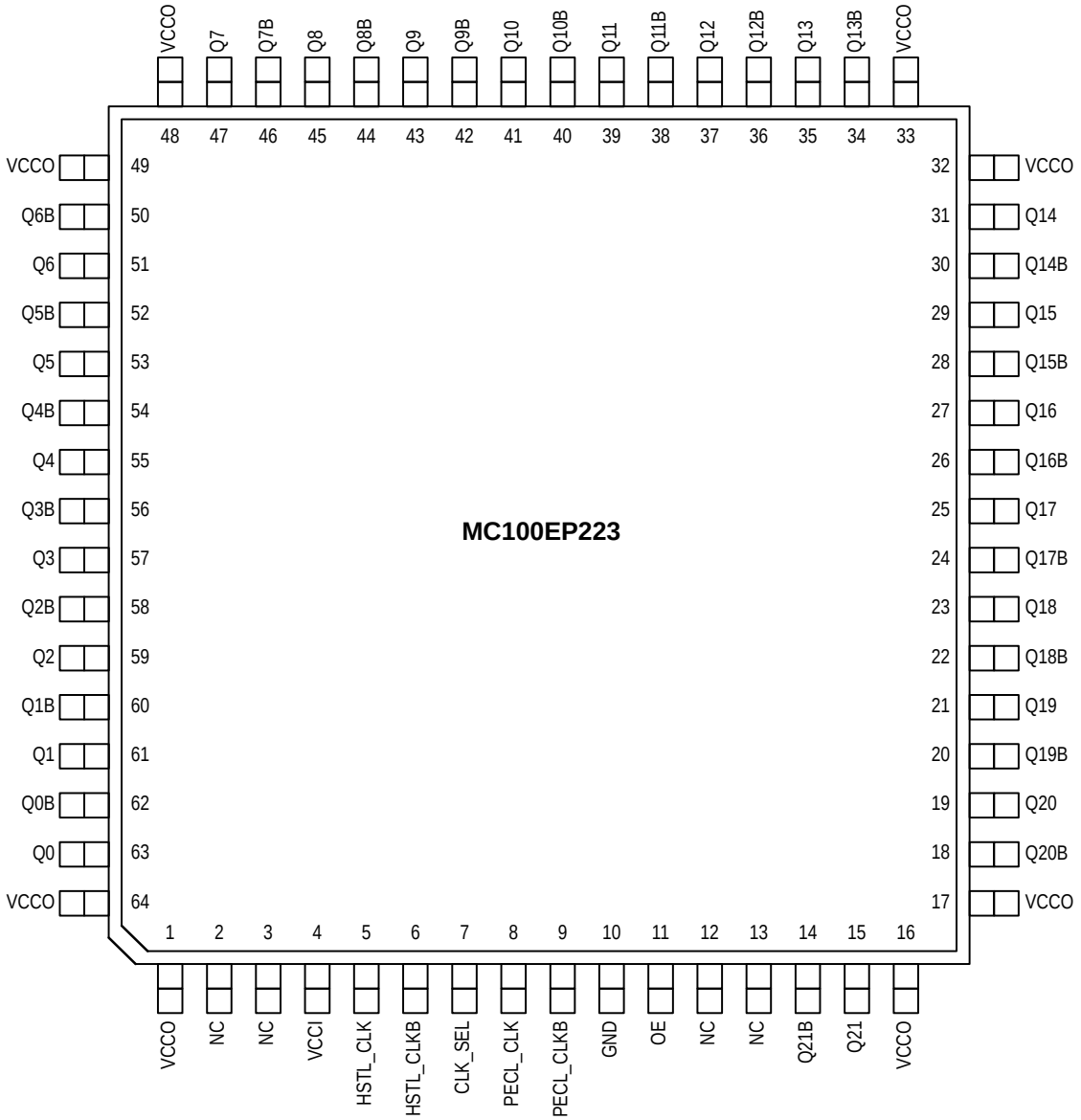


Figure 1. 64–Lead Pinout (Top View)

PIN NAMES

Pins	Function
HSTL_CLK, HSTL_CLKB	Differential HSTL Inputs
PECL_CLK, PECL_CLKB	Differential PECL Inputs
Q0:21, Q0B:21B	Differential HSTL Outputs
CLK_SEL	Active Clock Select Input
OE	Output Enable
GND	Ground
VCCI	Core VCC
VCCO	I/O VCC

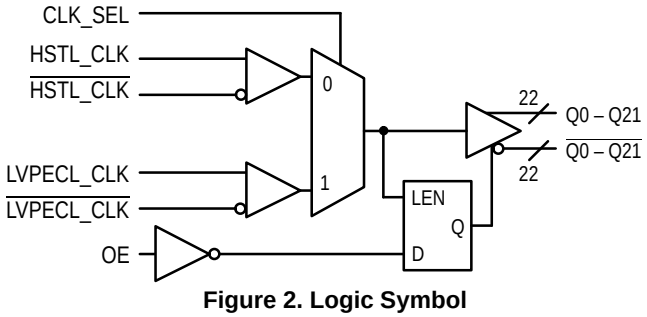


Figure 2. Logic Symbol

FUNCTION

OE	CLK_SEL	Q0:21, Q0B:21B
0	0	Q = Low, QB = High
0	1	Q = Low, QB = High
1	0	HSTL_CLK, HSTL_CLKB
1	1	PECL_CLK, PECL_CLKB

SIGNAL GROUPS

Level	Direction	Signal
HSTL	Input	HSTL_CLK, HSTL_CLKB
HSTL	Output	Q0:21, Q0B:21B
LVPECL	Input	PECL_CLK, PECL_CLKB
LVCMOS/LVTTL	Input	CLK_SEL, OE

HSTL DC CHARACTERISTICS

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage				1.0						V
V_{OL}	Output LOW Voltage						0.4				V
V_{IH}	Input HIGH Voltage				V_{CMR}+0.1		1.6				V
V_{IL}	Input LOW Voltage				–0.3		V_{CMR}–0.1				V
V_{CMR}	Input Crossover Voltage				0.68		0.9				V

PECL DC CHARACTERISTICS

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage (Note 1.)	2.135		2.420	2.135		2.420	2.135		2.420	V
V_{IL}	Input LOW Voltage (Note 1.)	1.490		1.825	1.490		1.825	1.490		1.825	V
I_{IH}	Input HIGH Current			150			150			150	μA

1. These values are for V_{CC} = 3.3V. Level specifications vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{EE} = GND, V_{CC} =$V_{CC(min)}$ to $V_{CC(max)}$)

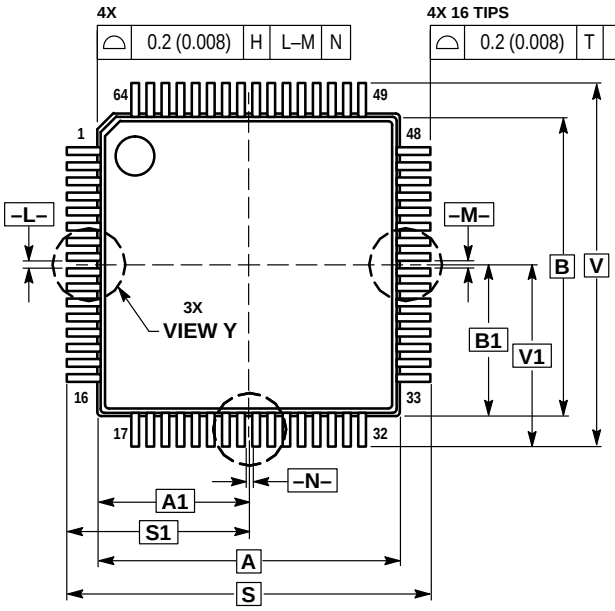
Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay to Output IN (Differential)		1.0			1.0			1.0		ns
t_{skew}	Within–Device Skew Part–to–Part Skew (Diff)			50 200			50 200			50 200	ps
f_{max}	Maximum Input Frequency			250			250			250	MHz
V_{PP}	Minimum Input Swing PECL_CLK		600			600			600		mV
V_{CMR}	Common Mode Range PECL_CLK										V
t_r, t_f	Output Rise/Fall Time (20–80%)	300		600	300		600	300		600	ps

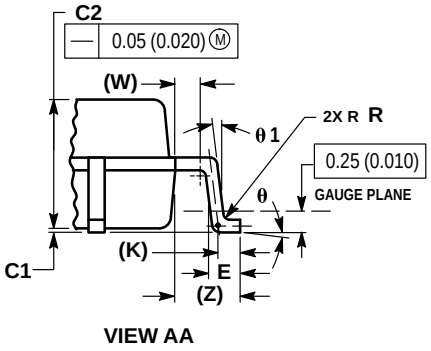
Power Supply Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
V_{CCI}	Core V_{CC}	3.0	3.3	3.6	V
V_{CCO}	I/O V_{CC}	1.6	1.8	2.0	V
I_{CC}	Power Supply Current				mA
I_{EE}	Power Supply Current				mA

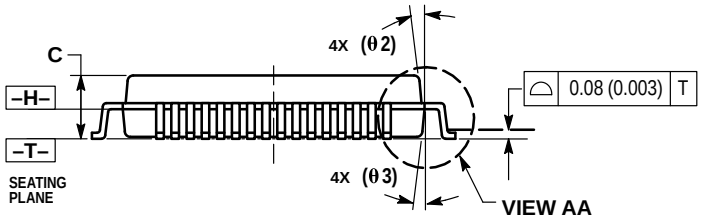
OUTLINE DIMENSIONS

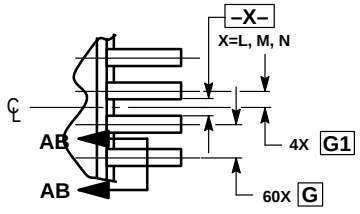
FA SUFFIX
PLASTIC TQFP PACKAGE
CASE 840F–02
ISSUE A



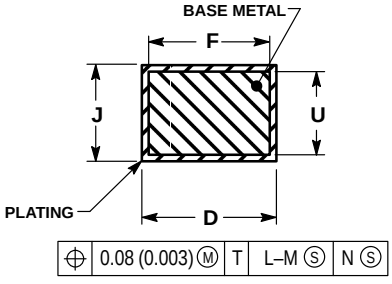


VIEW AA





VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE, –H– IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.35 (0.014). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B2	5.00 BSC		0.197 BSC	
C	—	1.60	—	0.063
C1	0.05	0.15	0.002	0.006
C2	1.35	1.45	0.053	0.057
D	0.17	0.27	0.007	0.011
E	0.45	0.75	0.018	0.030
F	0.17	0.23	0.007	0.009
G	0.50 BSC		0.020 BSC	
G1	0.25 BSC		0.010 BSC	
J	0.09	0.20	0.004	0.008
K	0.50 REF		0.020 REF	
R1	0.10	0.20	0.004	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12° REF		12° REF	
θ3	12° REF		12° REF	

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