D2825, DECEMBER 1983

- 10-Bit Versions of 'AS574 and 'AS576 with Improved $I_{OH}$ Specifications
- Ideal for Data Synchronization of Wider Data Paths
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Carriers in Addition to Plasstic and Ceramic DIPs
- Buffered Control Inputs to Reduce DC Loading Effects
- Dependable Texas Instruments Quality and Reliability

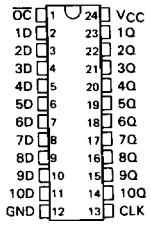
**description**

These 10-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

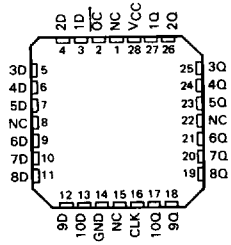
The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs on the 'AS821 will be true, and on the 'AS822 will be complementary, to the data input.

A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

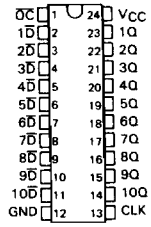
**SN54AS821 . . . JT PACKAGE**
**SN74AS821 . . . NT PACKAGE**
**(TOP VIEW)**



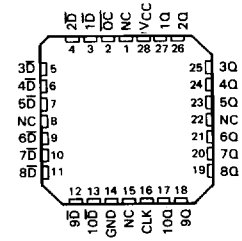

**SN54AS821 . . . FH PACKAGE**
**SN74AS821 . . . FN PACKAGE**
**(TOP VIEW)**




**SN54AS822 . . . JT PACKAGE**
**SN74AS822 . . . NT PACKAGE**
**(TOP VIEW)**




**SN54AS822 . . . FH PACKAGE**
**SN74AS822 . . . FN PACKAGE**
**(TOP VIEW)**




NC—No internal connection





**ADVANCE INFORMATION**

This document contains information on a new product. Specifications are subject to change without notice.





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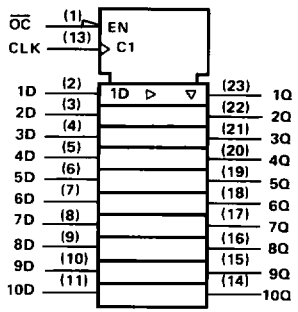
The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS821 and SN54AS822 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS821 and SN74AS822 are characterized for operation from 0°C to 70°C.

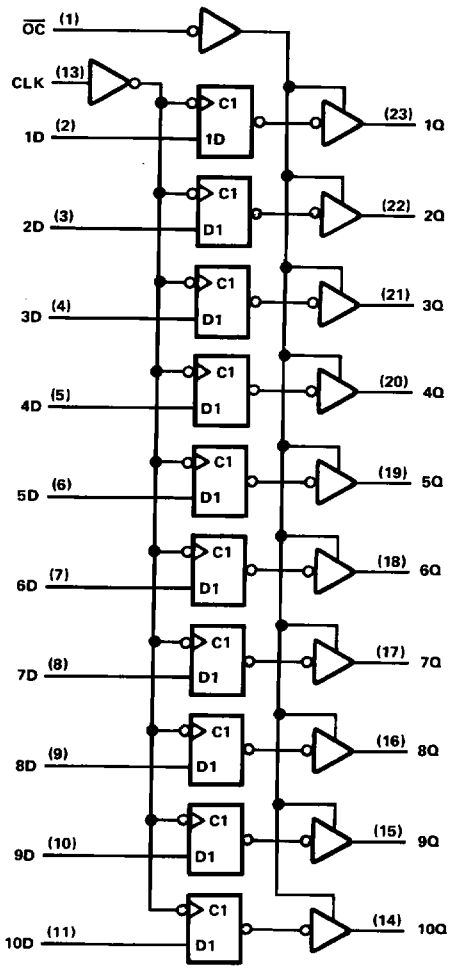
'AS821 FUNCTION TABLE (EACH FLIP-FLOP)

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OC}$ | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

'AS821 logic symbol




'AS821 logic diagram (positive logic)




Pin numbers shown are for JT and NT packages.





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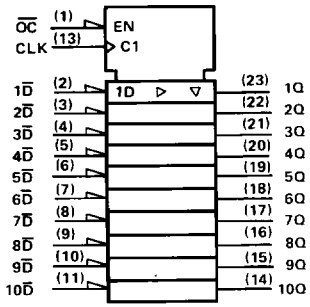
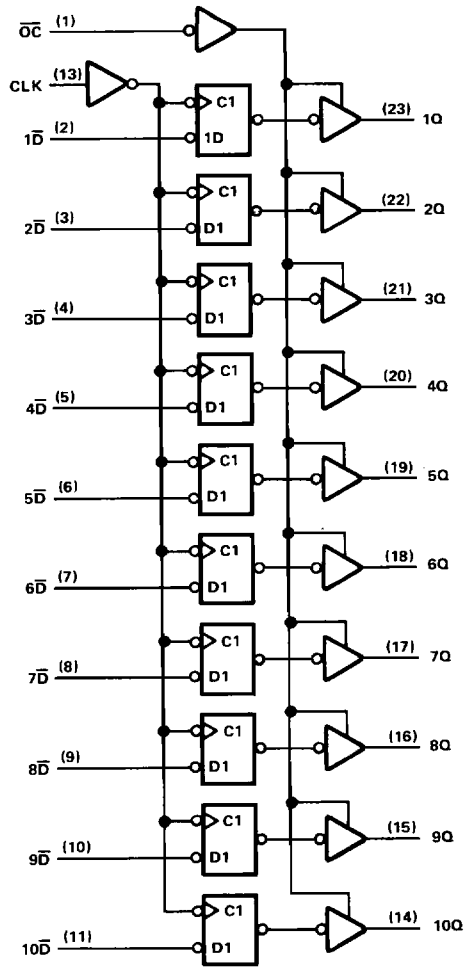
'AS822 FUNCTION TABLE (EACH FLIP-FLOP)

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OC}$ | CLK | $\overline{D}$ | Q |
| L | ↑ | H | L |
| L | ↑ | L | H |
| L | L | X | $Q_0$ |
| H | X | X | Z |

'AS822 logic symbol




'AS822 logic diagram (positive logic)




Pin numbers shown are for JT and NT packages

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS821, SN54AS822 . . . . . −55°C to 125°C
SN74AS821, SN74AS822 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

### recommended operating conditions

| | | SN54AS821 SN54AS822 | | | SN74AS821 SN74AS822 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −24 | | | −24 | mA |
| $I_{OL}$ | Low-level output current | | | 32 | | | 48 | mA |
| $t_w$ | Pulse duration, CLK high or low | 9 | | | 8 | | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | 7 | | | 6 | | | ns |
| $t_h$ | Hold time, data after CLK↑ | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54AS821 SN54AS822 | | | SN74AS821 SN74AS822 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −2 mA | $V_{CC}$−2 | | | $V_{CC}$−2 | | | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −15 mA | 2.4 | 3.2 | | 2.4 | 3.2 | | |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −24 mA | 2 | | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 32 mA | | 0.25 | 0.5 | | | | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 48 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | μA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | −50 | | | −50 | μA |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.5 | | | −0.5 | mA |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −30 | | −112 | −30 | | −112 | mA |
| $I_{CC}$ | 'AS821 | $V_{CC}$ = 5.5 V | Outputs high | | 55 | 88 | | 55 | 88 | mA |
| | | | Outputs low | | 68 | 109 | | 68 | 109 | |
| | | | Outputs disabled | | 70 | 113 | | 70 | 113 | |
| | 'AS822 | | Outputs high | | 55 | 88 | | 55 | 88 | |
| | | | Outputs low | | 68 | 109 | | 68 | 109 | |
| | | | Outputs disabled | | 70 | 113 | | 70 | 113 | |

†All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.





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## switching characteristics (see Note 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54AS821 SN54AS822 | | SN74AS821 SN74AS822 | | |
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | CLK | Any Q | 3.5 | 9 | 3.5 | 7.5 | ns |
| $t_{PHL}$ | | | 3.5 | 11.5 | 3.5 | 10.5 | |
| $t_{PZH}$ | $\overline{OC}$ | Any Q | 4 | 12 | 4 | 11 | ns |
| $t_{PZL}$ | | | 4 | 13 | 4 | 12 | |
| $t_{PHZ}$ | $\overline{OC}$ | Any Q | 2 | 10 | 2 | 8 | ns |
| $t_{PZL}$ | | | 2 | 10 | 2 | 8 | |

NOTE 1: For load circuit and voltage waveforms, see page 1-12.