

Octal inverting buffer with 30Ω series termination resistors (3-State)

74ABT240-1

FEATURES

- Octal bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Outputs include series resistance of 30W, making external termination resistors unnecessary
- Output capability: +12mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State

DESCRIPTION

The 74ABT240-1 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT240-1 device is an octal inverting buffer that is ideal for driving bus lines. The device features two Output Enables (1OE, 2OE), each controlling four of the 3-State outputs.

The 74ABT240-1 is designed with 30W series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	$C_L = 50\text{pF}; V_{CC} = 5\text{V}$	3.5	ns
C_{IN}	Input capacitance	$V_I = 0\text{V or } V_{CC}$	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_O = 0\text{V or } V_{CC}$	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	50	μA

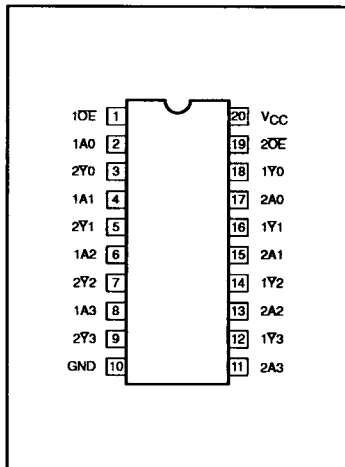
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	-40°C to +85°C	74ABT240-1N	0408B
20-pin plastic SOL	-40°C to +85°C	74ABT240-1D	0172D
20-pin SSOP Type II	-40°C to +85°C	74ABT240-1DB	1640A

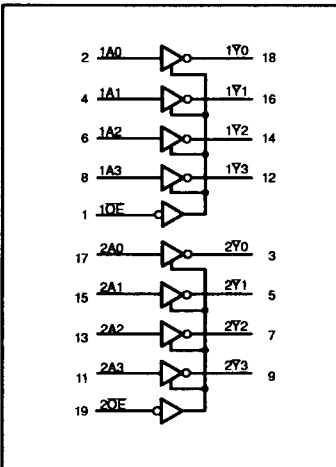
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 - 1A3	Data inputs
11, 13, 15, 17	2A0 - 2A3	Data inputs
18, 16, 14, 12	1Y0 - 1Y3	Data outputs
9, 7, 5, 3	2Y0 - 2Y3	Data outputs
1, 19	1OE, 2OE	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

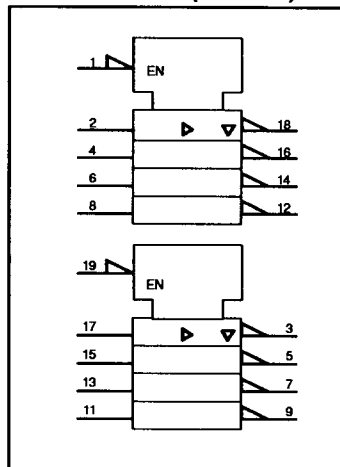
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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FUNCTION TABLE

INPUTS				OUTPUTS	
1OE	1An	2OE	2An	1Yn	2Yn
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

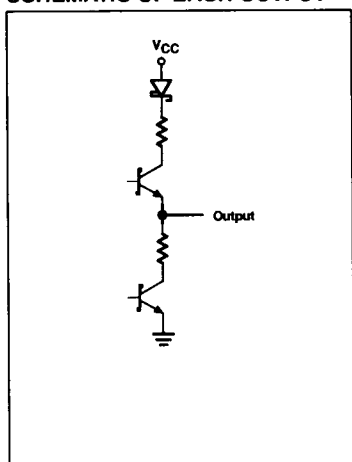
H = High voltage level

L = Low voltage level

X = Don't care

Z = High impedance "off" state

SCHEMATIC OF EACH OUTPUT



ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level Input voltage		0.8	V
I _{OH}	High-level output current		-32	mA
I _{OL}	Low-level output current		12	mA
ΔV/ΔV	Input transition rise or fall rate	0	5	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA		-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 5mA; V _I = V _{IL} or V _{IH} ;	0.32	0.55		0.55		V
		V _{CC} = 4.5V; I _{OL} = 12mA; V _I = V _{IL} or V _{IH} ;			0.8	0.8		V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V	±0.01	±1.0		±1.0		μA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V	±5.0	±100		±100		μA
I _{PUPD}	Power-up/down 3-State output current ³	V _{CC} = 2.1V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = Don't care	±5.0	±50		±50		μA
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}	0.01	50		50		μA
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}	-0.01	-50		-50		μA
I _{CEx}	Output high leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}	5.0	50		50		μA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V	-50	-100	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}	50	250		250		μA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}	24	30		30		mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}	50	50		50		μA
ΔI _{CC}	Additional supply current per input pin ²	Outputs 3-State, one enable input at 3.4V, other inputs at V _{CC} or GND; V _{CC} = 5.5V	0.5	1.5		1.5		mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100μsec is permitted.

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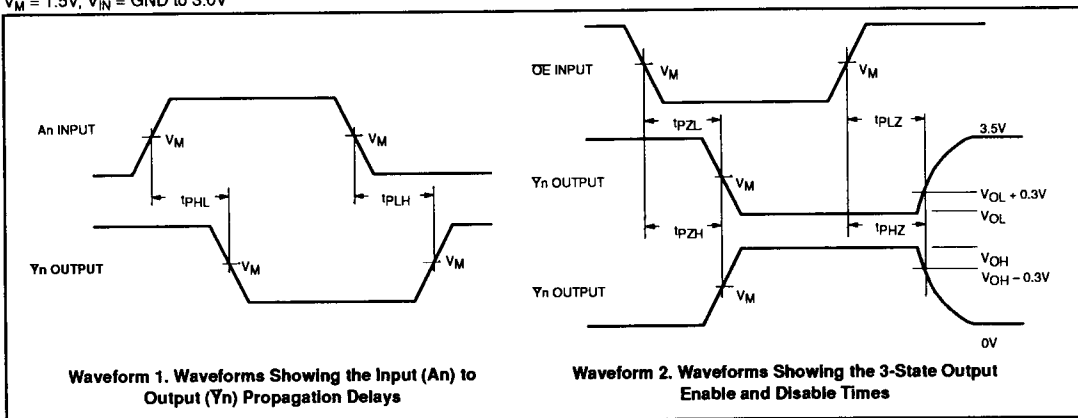
AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$			$T_{\text{amb}} = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to \bar{Y}_n	1	1.0 1.9	2.9 3.5	4.1 4.8	1.0 1.9	4.8 5.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 1.4	3.1 3.2	4.4 4.7	1.1 1.4	5.2 5.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.5 2.4	4.8 4.7	6.1 6.0	2.5 2.4	6.7 6.5	ns

AC WAVEFORMS

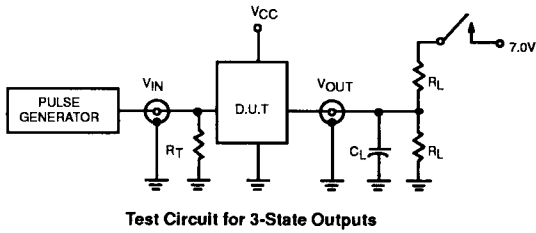
$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



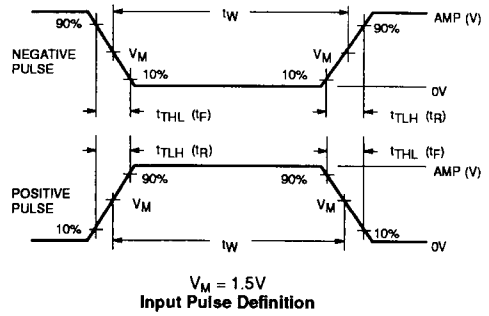
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TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns