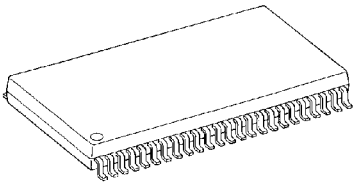
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74LCX16240AFT

LOW-VOLTAGE 16-BIT BUS BUFFER (INVERTED) WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX16240AFT is a high performance CMOS 16bit BUS BUFFER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.
This device is inverting 3 – state buffer having four active – low output enables. It can be used as four 4-bit buffers two 8-bit buffers or one 16-bit buffer. When the $\overline{OE}$ input is high, the outputs are in a high impedance state. This device is designed to be used with 3 – state memory address drivers, etc.
All inputs are equipped with protection circuits against static discharge.



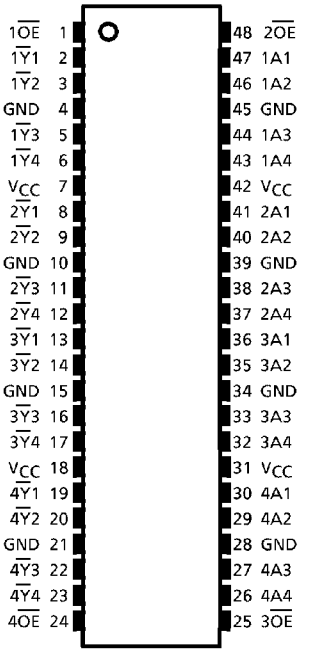
TSSOP48-P-0061-0.50

Weight : 0.25g (Typ.)

FEATURES

- Low Voltage Operation : $V_{CC} = 2.0 \sim 3.6V$
- High Speed Operation : $t_{pd} = 4.9ns$ (max.) at $V_{CC} = 3.0 \sim 3.6V$
- Output Current : $|I_{OH}| / I_{OL} = 24mA$ (MIN) at $V_{CC} = 3.0V$
- Latch-up Performance : ±500mA
- Package : TSSOP
  (Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.

PIN CONNECTION



(TOP VIEW)

961001EBA2

TRUTH TABLE

INPUTS		OUTPUTS
$1\overline{OE}$	1A1-1A4	$1\overline{Y}1$-$1\overline{Y}4$
L	L	H
L	H	L
H	X	Z

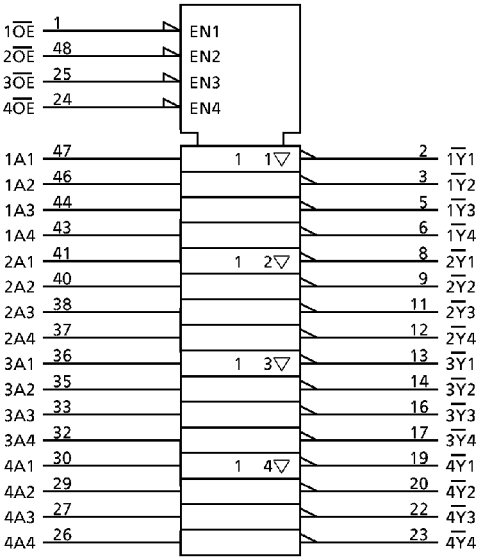
INPUTS		OUTPUTS
$2\overline{OE}$	2A1-2A4	$2\overline{Y}1$-$2\overline{Y}4$
L	L	H
L	H	L
H	X	Z

INPUTS		OUTPUTS
$3\overline{OE}$	3A1-3A4	$3\overline{Y}1$-$3\overline{Y}4$
L	L	H
L	H	L
H	X	Z

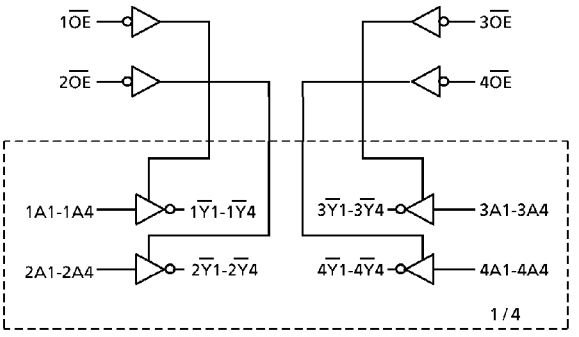
INPUTS		OUTPUTS
$4\overline{OE}$	4A1-4A4	$4\overline{Y}1$-$4\overline{Y}4$
L	L	H
L	H	L
H	X	Z

X : Don't Care
Z : High impedance

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



961001EBA2'

MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	−0.5~7.0	V
Input Voltage	V_{IN}	−0.5~7.0	V
Output Voltage	V_{OUT}	−0.5~7.0 (Note 1)	V
		−0.5~V_{CC}+0.5 (Note 2)	
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	I_{OK}	±50 (Note 3)	mA
DC Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	400	mW
DC V_{CC} / Ground Current Per Supply Pin	I_{CC} / I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

(Note 1) Off-State

(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.

(Note 3) V_{OUT}<GND, V_{OUT}>V_{CC}

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
		1.5~3.6 (Note 4)	
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5 (Note 5)	V
		0~ V_{CC} (Note 6)	
Output Current	I_{OH} / I_{OL}	±24 (Note 7)	mA
		±12 (Note 8)	
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt / dv	0~10 (Note 9)	ns / V

(Note 4) Data Retention Only

(Note 5) Off-State

(Note 6) High or Low State

(Note 7) V_{CC} = 3.0~3.6V

(Note 8) V_{CC} = 2.7~3.0V

(Note 9) V_{IN} = 0.8~2.0V, V_{CC} = 3.0V

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = −40~85°C)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN.	MAX.	UNIT
Input Voltage	"H" Level	V_{IH}			2.7~3.6	2.0	—	V
	"L" Level	V_{IL}			2.7~3.6	—	0.8	V
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100μA	2.7~3.6	V_{CC} −0.2	—	V
				I_{OH} = −12μA	2.7	2.2	—	
				I_{OH} = −18mA	3.0	2.4	—	
				I_{OH} = −24mA	3.0	2.2	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100μA	2.7~3.6	—	0.2	V
				I_{OL} = 12mA	2.7	—	0.4	
				I_{OL} = 16mA	3.0	—	0.4	
				I_{OL} = 24mA	3.0	—	0.55	
Input Leakage Current		I_{IN}	V_{IN} = 0~5.5V		2.7~3.6	—	±5.0	μA
3-State Output Off-State Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~5.5V		2.7~3.6	—	±5.0	μA
Power Off Leakage Current		I_{OFF}	V_{IN} / V_{OUT} = 5.5V		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	—	20.0	μA
			V_{IN} / V_{OUT} = 3.6~5.5V		2.7~3.6	—	±20.0	
Increase In I_{CC} Per Input		ΔI_{CC}	V_{IH} = V_{CC} − 0.6V		2.7~3.6	—	500	μA

AC characteristics (Ta = – 40~85°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{CC} (V)	MIN.	MAX.	UNIT
Propagation Delay Time	t_{pLH} t_{pHL}	(Fig.1, 2)	2.7	—	5.9	ns
			3.3 ± 0.3	1.5	4.9	
3-State Output Enable Time	t_{pZL} t_{pZH}	(Fig.1, 3)	2.7	—	7.5	ns
			3.3 ± 0.3	1.5	6.5	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	(Fig.1, 3)	2.7	—	6.5	ns
			3.3 ± 0.3	1.5	5.5	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 10)	2.7	—	—	ns
			3.3 ± 0.3	—	1.0	

(Note 10) Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Dynamic switching characteristics
(Ta = 25°C, Input $t_r = t_f = 2.5$ns, $C_L = 50$pF, $R_L = 500\Omega$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$V_{IH} = 3.3$V, $V_{IL} = 0$V	3.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	$\|V_{OLV}\|$	$V_{IH} = 3.3$V, $V_{IL} = 0$V	3.3	0.8	V

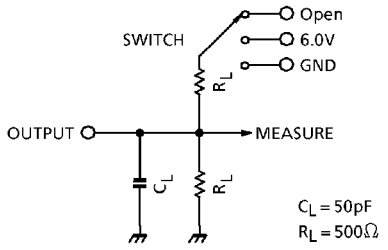
Capacitive characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP	UNIT
Input Capacitance	C_{IN}	—	3.3	7	pF
Output Capacitance	C_{OUT}		3.3	8	pF
Power Dissipation Capacitance	C_{PD}	$f_{IN} = 10$MHz (Note 11)	3.3	25	pF

(Note 11) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

$I_{CC (opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 16$. (Per bit)

Fig.1 Test circuit



PARAMETER	SWITCH
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0V
t_{pHZ}, t_{pZH}	GND

AC WAVEFORM

Fig.2 t_{pLH}, t_{pHL}

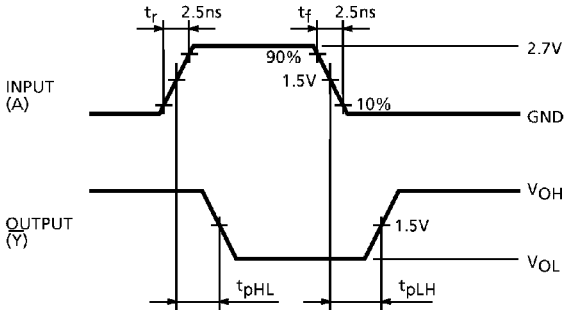
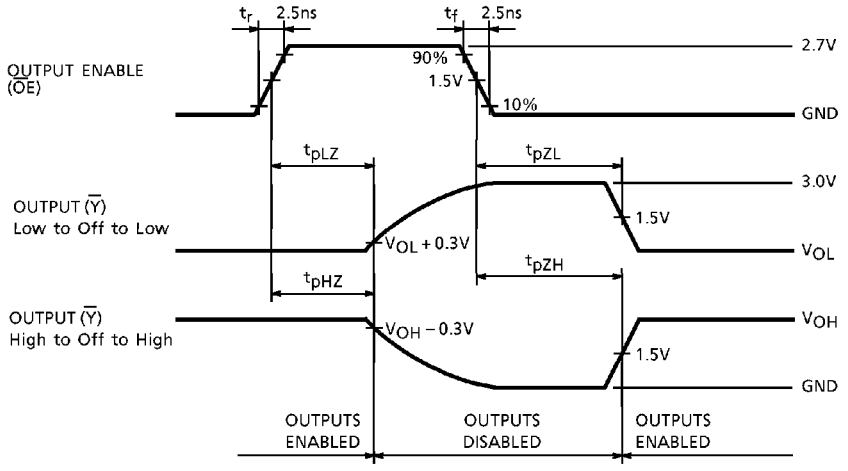
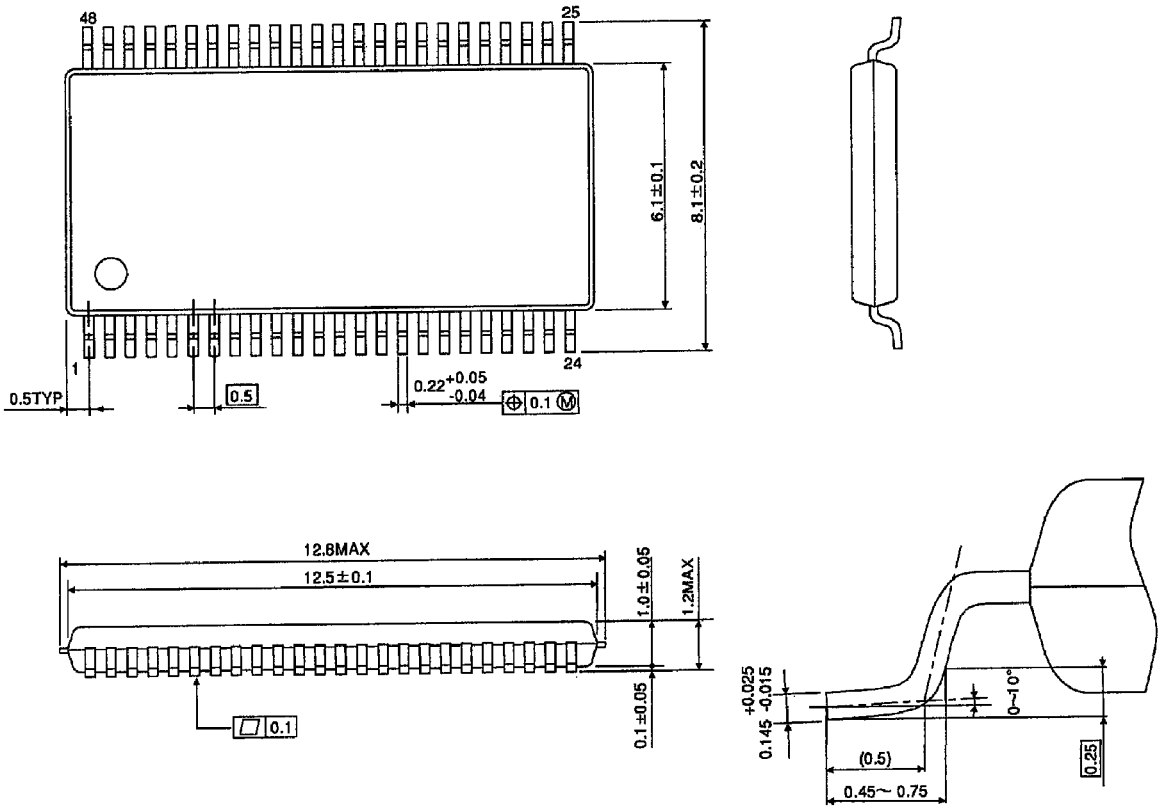


Fig.3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}



OUTLINE DRAWING

TSSOP48-P-0061-0.50 Unit : mm



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