

SN54HC533, SN74HC533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- 8 Latches in a Single Package
- High-Current 3-State Inverting Outputs Can Drive Up to 15 LSTTL Loads
- Full Parallel Access for Loading
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

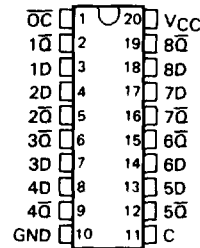
The eight latches of the 'HC533 are transparent D-type latches. While the enable (C) is high, the \bar{Q} outputs will follow the complements of the D inputs. When the enable is taken low, the \bar{Q} outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'HC533 is functionally equivalent to the 'HC373 except for having inverted outputs.

An output-control (\bar{OC}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

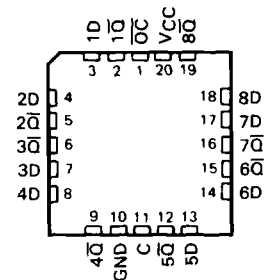
The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54HC533 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC533 is characterized for operation from -40°C to 85°C .

SN54HC533 . . . J PACKAGE
SN74HC533 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC533 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
\bar{OC}	ENABLE C	D	\bar{Q}
L	H	H	L
L	H	L	H
L	L	X	\bar{Q}_0
H	X	X	Z

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PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

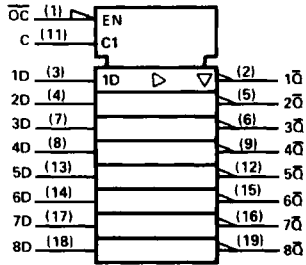
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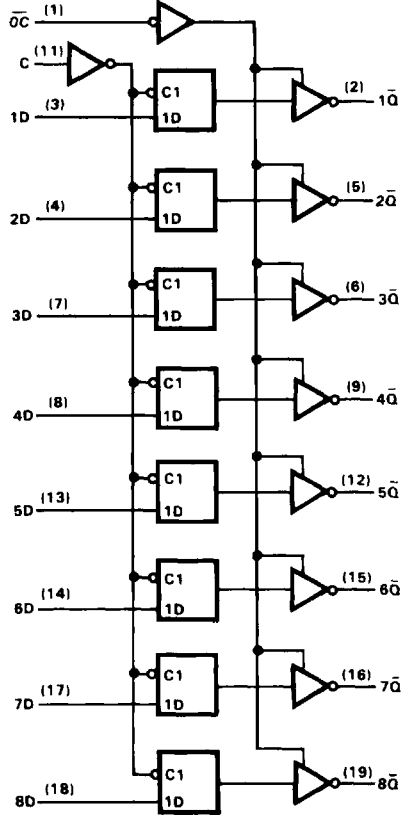
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logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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HCMS Devices

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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND pins	± 70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package	260°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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HCMOS Devices

recommended operating conditions

		SN54HC533			SN74HC533			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5	$V_{CC} = 2$ V		1.5	V
		$V_{CC} = 4.5$ V		3.15	$V_{CC} = 4.5$ V		3.15	
		$V_{CC} = 6$ V		4.2	$V_{CC} = 6$ V		4.2	
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0	$V_{CC} = 2$ V		0	V
		$V_{CC} = 4.5$ V		0	$V_{CC} = 4.5$ V		0	
		$V_{CC} = 6$ V		0	$V_{CC} = 6$ V		0	
V_I	Input voltage	0	V_{CC}		0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		0	V_{CC}		V
t_t	Input transition (rise and fall) times	$V_{CC} = 2$ V		0	$V_{CC} = 2$ V		1000	ns
		$V_{CC} = 4.5$ V		0	$V_{CC} = 4.5$ V		500	
		$V_{CC} = 6$ V		0	$V_{CC} = 6$ V		400	
T_A	Operating free-air temperature	-55	125		-40	85		°C



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**SN54HC533, SN74HC533
OCTAL D-TYPE TRANSPARENT LATCHES
WITH 3-STATE OUTPUTS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25 °C			SN54HC533		SN74HC533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL} , I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V _I = V _{IH} or V _{IL} , I _{OH} = -6 mA	4.5 V	3.98	4.30		3.7		3.84		
V _I = V _{IH} or V _{IL} , I _{OH} = -7.8 mA	6 V	5.48	5.80		5.2		5.34			
V _{OL}	V _I = V _{IH} or V _{IL} , I _{OL} = 20 μA	2 V	0.002	0.1		0.1		0.1	V	
		4.5 V	0.001	0.1		0.1		0.1		
		6 V	0.001	0.1		0.1		0.1		
	V _I = V _{IH} or V _{IL} , I _{OL} = 6 mA	4.5 V	0.17	0.26		0.4		0.33		
V _I = V _{IH} or V _{IL} , I _{OL} = 7.8 mA	6 V	0.15	0.26		0.4		0.33			
I _I	V _I = V _{CC} or 0	6 V	±0.1	±100		±1000		±1000	nA	
I _{OZ}	V _O = V _{CC} or 0	6 V	±0.01	±0.5		±10		±5	μA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V		8		160		80	μA	
C _i		2 to 6 V		3	10		10		10	pF

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HC MOS Devices

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V _{CC}	T _A = 25 °C		SN54HC533		SN74HC533		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w Pulse duration, enable C high	2 V	80		120		100		ns
	4.5 V	16		24		20		
	6 V	14		20		17		
t _{su} Setup time, data before enable C↓	2 V	50		75		63		ns
	4.5 V	10		15		13		
	6 V	9		13		11		
t _h Hold time, data after enable C↓	2 V	20		26		24		ns
	4.5 V	10		13		12		
	6 V	10		13		12		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25 °C			SN54HC533		SN74HC533		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	D	Q̄	2 V	77	150		225		185	ns	
			4.5 V	26	30		45		38		
			6 V	23	26		38		32		
t _{pd}	C	Any Q̄	2 V	87	175		265		220	ns	
			4.5 V	27	35		53		44		
			6 V	23	30		45		38		
t _{en}	Q̄C	Any Q̄	2 V	68	150		225		190	ns	
			4.5 V	24	30		45		38		
			6 V	21	26		38		32		
t _{dis}	Q̄C	Any Q̄	2 V	47	150		225		190	ns	
			4.5 V	23	30		45		38		
			6 V	21	26		38		32		
t _t		Any Q̄	2 V	28	60		90		75	ns	
			4.5 V	8	12		18		15		
			6V	6	10		15		13		

C _{pd}	Power dissipation capacitance per latch	No load, T _A = 25 °C	50 pF typ
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Note 1: Load circuits and voltage waveforms are shown in Section 1.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L = 150$ pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC533		SN74HC533		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	D	\bar{Q}	2 V		95	200		300		250	ns
			4.5 V		33	40		60		50	
			6 V		21	34		51		43	
t _{pd}	C	Any \bar{Q}	2 V		103	225		335		280	ns
			4.5 V		33	45		67		56	
			6 V		29	38		57		48	
t _{en}	\bar{OC}	Any \bar{Q}	2 V		85	200		300		250	ns
			4.5 V		29	40		60		50	
			6 V		28	34		51		43	
t _t		Any \bar{Q}	2 V		60	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		14	38		53		45	

Note 1: Load circuits and voltage waveforms are shown in Section 1.