

**OCTAL BUS TRANSCEIVER; 3-STATE; TRUE/INVERTING**

**FEATURES**

- Octal bidirectional bus interface
- True and inverting 3-state outputs
- Output capability: bus driver
- ICC category: MSI

**GENERAL DESCRIPTION**

The 74HC/HCT643 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT643 are octal transceivers featuring true and inverting 3-state bus compatible outputs in both send and receive directions.

The "643" features an output enable ( $\overline{OE}$ ) input for easy cascading and a send/receive (DIR) for direction control.  $\overline{OE}$  controls the outputs so that the buses are effectively isolated.

**FUNCTION TABLE**

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A <sub>n</sub>	B <sub>n</sub>
L	L	A = B	inputs
L	H	inputs	B = $\overline{A}$
H	X	Z	Z

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; inverting B <sub>n</sub> to A <sub>n</sub> ; true	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	7 8	8 11	ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>I/O</sub>	input/output capacitance		10	10	pF
CPD	power dissipation capacitance per transceiver	notes 1 and 2	42	44	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

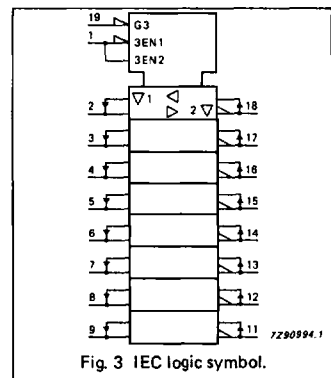
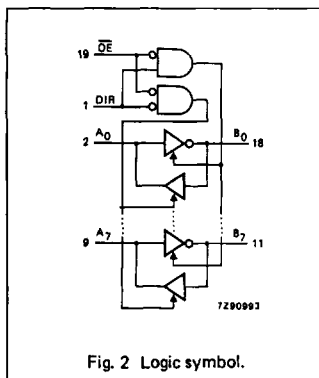
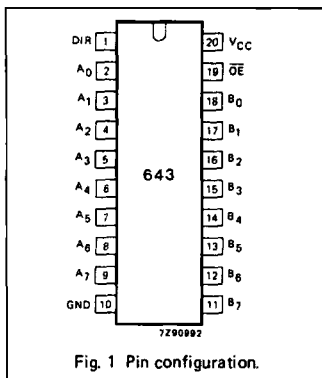
- CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  
 $P_D = CPD \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
- For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

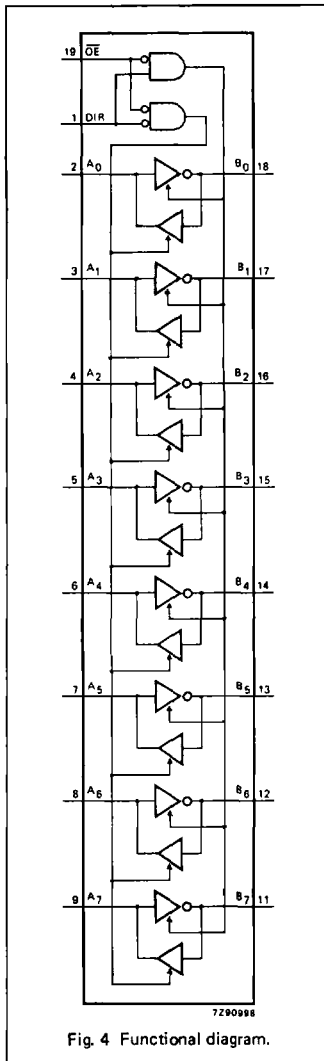
**PACKAGE OUTLINES**

SEE PACKAGE INFORMATION SECTION

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A <sub>0</sub> to A <sub>7</sub>	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B <sub>0</sub> to B <sub>7</sub>	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V <sub>CC</sub>	positive supply voltage





## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; inverting		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 5
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay B <sub>n</sub> to A <sub>n</sub> ; non-inverting (true)		28 10 8	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE, DIR to A <sub>n</sub> ; OE, DIR to B <sub>n</sub>		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE, DIR to A <sub>n</sub> ; OE, DIR to B <sub>n</sub>		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 5 and 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
A <sub>n</sub>	1.50
B <sub>n</sub>	0.40
OE	1.50
DIR	0.90

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; inverting		10	20		25		30	ns	4.5	Fig. 5
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay B <sub>n</sub> to A <sub>n</sub> ; non-inverting (true)		13	23		29		35	ns	4.5	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE, DIR to A <sub>n</sub> ; OE, DIR to B <sub>n</sub>		16	30		38		45	ns	4.5	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE, DIR to A <sub>n</sub> ; OE, DIR to B <sub>n</sub>		17	30		38		45	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Figs 5 and 6

AC WAVEFORMS

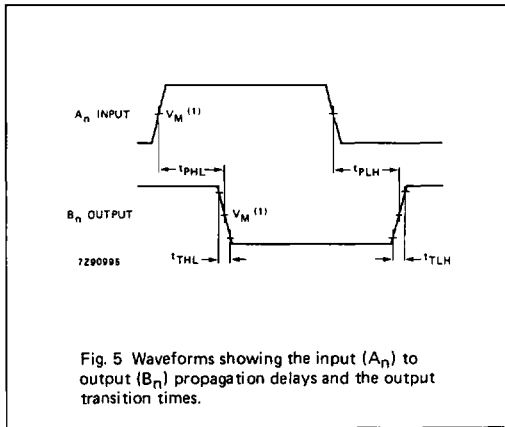


Fig. 5 Waveforms showing the input ( $A_n$ ) to output ( $B_n$ ) propagation delays and the output transition times.

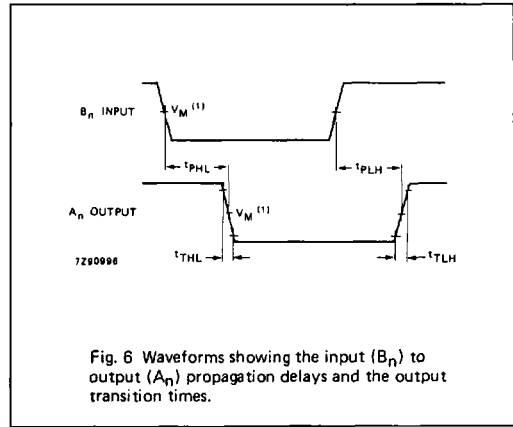


Fig. 6 Waveforms showing the input ( $B_n$ ) to output ( $A_n$ ) propagation delays and the output transition times.

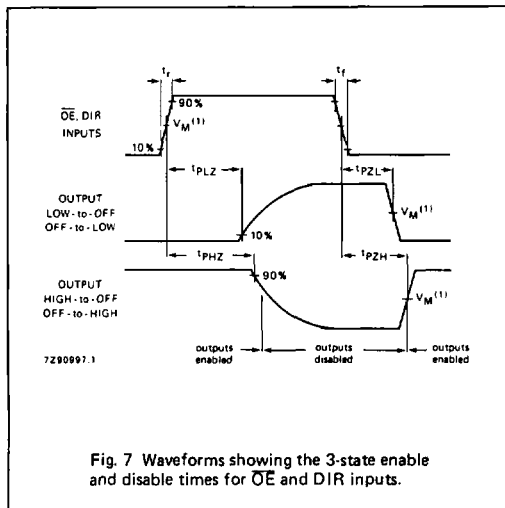


Fig. 7 Waveforms showing the 3-state enable and disable times for  $\overline{OE}$  and DIR inputs.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .