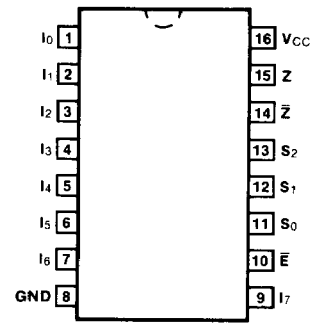


Ref 83125 }
 Dm 9312 }
 9312 010171 ✓
 93L12 016624 ✓
93S12 010259

8-INPUT MULTIPLEXER

CONNECTION DIAGRAM
PINOUT A



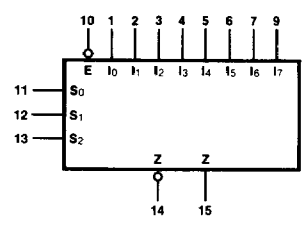
DESCRIPTION — The '12 is a monolithic, high speed, 8-input digital multiplexer circuit. It provides, in one package, the ability to select one bit of data from up to eight sources. The '12 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- FULLY BUFFERED COMPLEMENTARY OUTPUTS

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	9312PC, 93L12PC 93S12PC		9B
Ceramic DIP (D)	A	9312DC, 93L12DC 93S12DC	9312DM, 93L12DM 93S12DM	6B
Flatpak (F)	A	9312FC, 93L12FC 93S12FC	9312FM, 93L12FM 93S12FM	4L

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93S (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
S ₀ — S ₂	Select Inputs	1.0/1.0	1.25/1.25	0.5/0.25
E	Enable Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
I ₀ — I ₇	Multiplexer Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Z	Multiplexer Output	20/10	25/12.5	10/5.0 (3.0)
Z-bar	Complementary Multiplexer Output	20/10	25/12.5	10/5.0 (3.0)

FUNCTIONAL DESCRIPTION — The '12 is a logical implementation of a single pole, eight position switch with the switch position controlled by the state of three Select inputs, S₀, S₁, S₂. Both assertion and negation outputs are provided. The Enable input (E) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW, regardless of all other inputs. The logic function provided at the output is:

$$Z = E \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

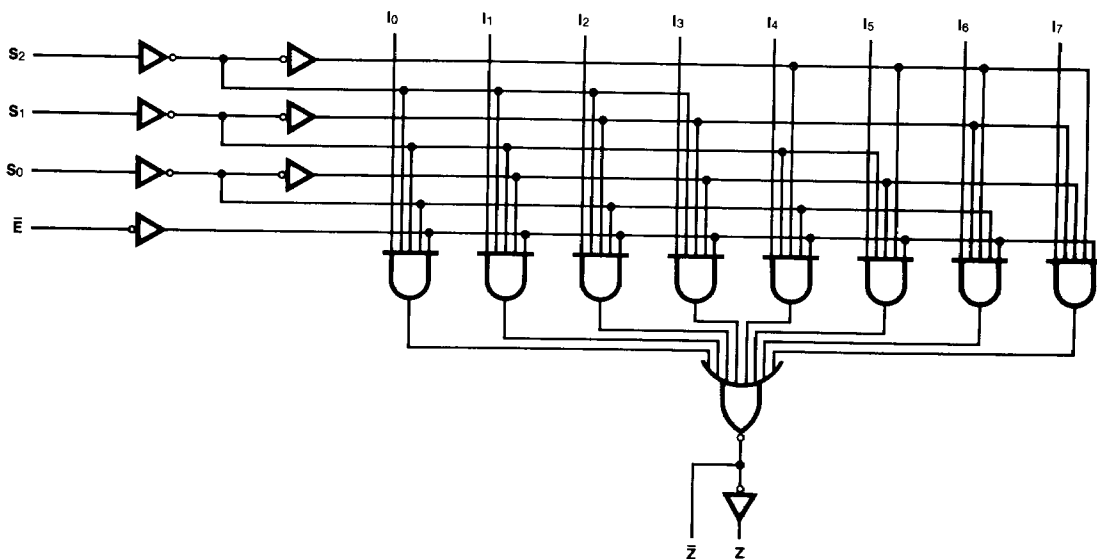
The '12 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the '12 can provide any logic function of four variables and its negation. Thus any number of random logic elements used to generate unusual truth tables can be replaced by one '12.

TRUTH TABLE

INPUTS												OUTPUTS	
\bar{E}	S ₂	S ₁	S ₀	I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	\bar{Z}	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

LOGIC DIAGRAM



6

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93S		93L		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I _{CC}	Power Supply Current	44		62		13.3		mA	V _{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93S		93L		UNITS	CONDITIONS
		C _L = 15 pF		C _L = 15 pF		C _L = 15 pF			
		Min	Max	Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay S ₀ to Z	34	34	17	18	60	75	ns	Figs. 3-1, 3-5
t _{PLH} t _{PHL}	Propagation Delay S ₀ to Z̄	24	26	16	15	45	65	ns	Figs. 3-1, 3-4
t _{PLH} t _{PHL}	Propagation Delay Ē to Z	30	30	13	16	50	70	ns	Figs. 3-1, 3-4
t _{PLH} t _{PHL}	Propagation Delay Ē to Z̄	20	23	14	11	35	60	ns	Figs. 3-1, 3-5
t _{PLH} t _{PHL}	Propagation Delay I _n to Z	24	24	12	12	60	55	ns	Figs. 3-1, 3-5
t _{PLH} t _{PHL}	Propagation Delay I _n to Z̄	14	16	8.0	9.0	45	45	ns	Figs. 3-1, 3-4