



# FAST CMOS 16-BIT BUS TRANSCEIVER/ REGISTER (3-STATE)

**IDT74FCT16646AT/CT/ET**

## FEATURES:

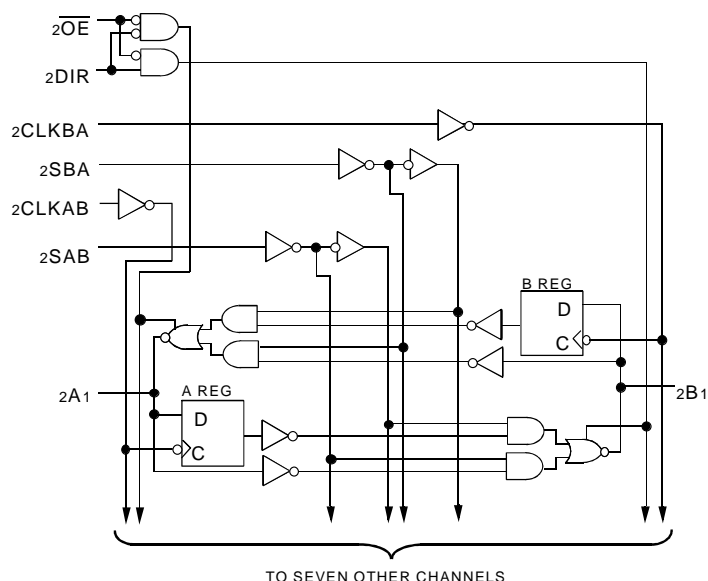
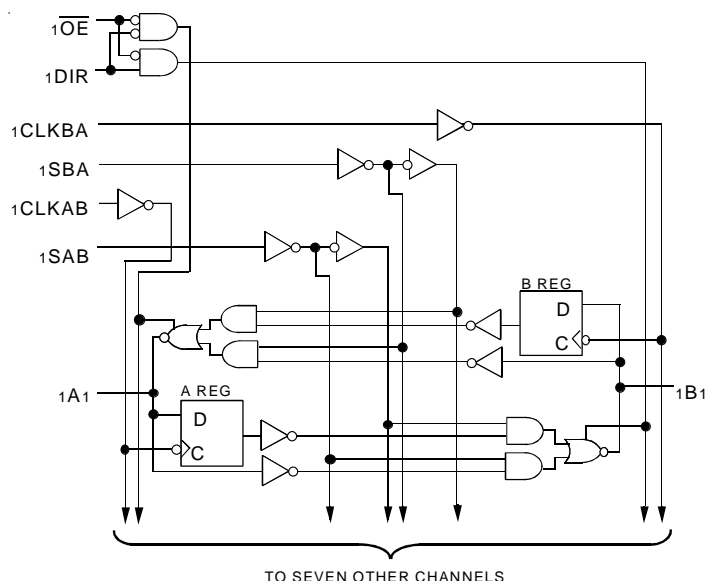
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- Low input and output leakage  $\leq 1\mu A$  (max.)
- $V_{CC} = 5V \pm 10\%$
- High drive outputs (-32mA  $I_{OH}$ , 64mA  $I_{OL}$ )
- Power off disable outputs permit "live insertion"
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1.0V at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$
- Available in SSOP and TSSOP packages

## DESCRIPTION:

The FCT16646T 16-bit registered transceiver is built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit bus transceivers with 3-state D-type registers. The control circuitry is organized for multiplexed transmission of data between A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/register features direction control (xDIR), over-riding Output Enable control (x $\overline{OE}$ ) and Select lines (xSAB and xSBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the low-to-high transitions at the appropriate clock pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

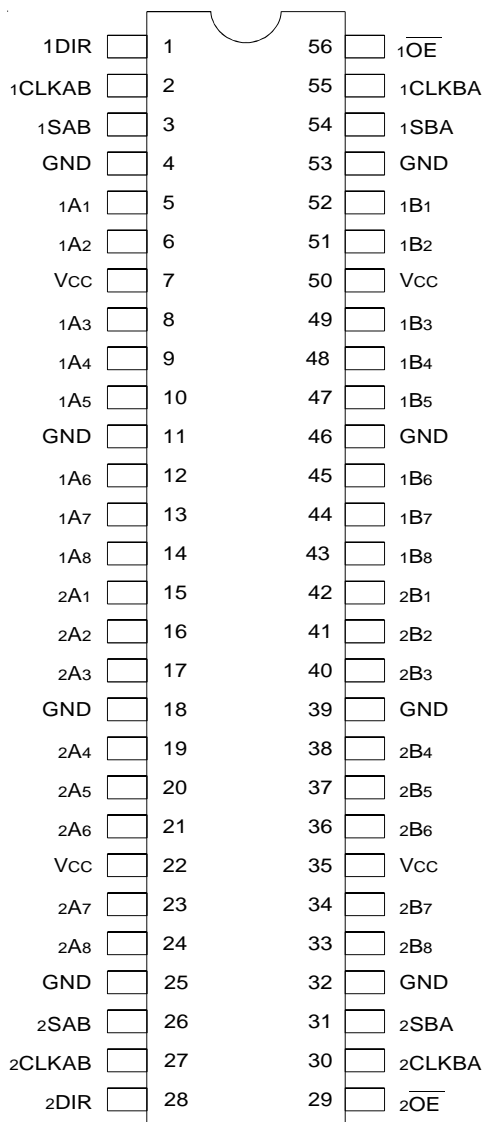
The FCT16646T is ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

## FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION



SSOP/ TSSOP  
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

| Symbol               | Description                          | Max             | Unit |
|----------------------|--------------------------------------|-----------------|------|
| VTERM <sup>(2)</sup> | Terminal Voltage with Respect to GND | -0.5 to +7      | V    |
| VTERM <sup>(3)</sup> | Terminal Voltage with Respect to GND | -0.5 to Vcc+0.5 | V    |
| TSTG                 | Storage Temperature                  | -65 to +150     | °C   |
| IOUT                 | DC Output Current                    | -60 to +120     | mA   |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX Output and I/O terminals.
- Output and I/O terminals for FCT162XXX.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

| Symbol | Parameter <sup>(1)</sup> | Conditions | Typ. | Max. | Unit |
|--------|--------------------------|------------|------|------|------|
| CIN    | Input Capacitance        | VIN = 0V   | 3.5  | 6    | pF   |
| COUT   | Output Capacitance       | VOUT = 0V  | 3.5  | 8    | pF   |

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

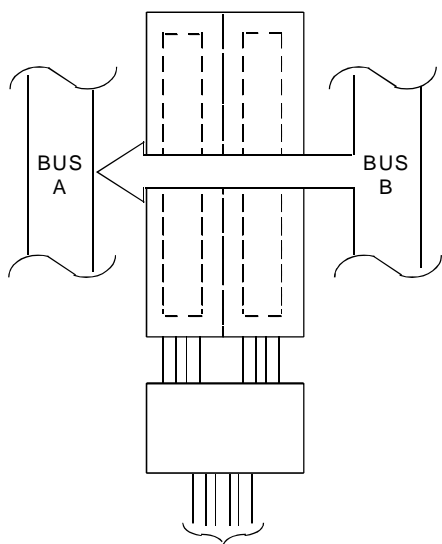
| Pin Names      | Description                                       |
|----------------|---|
| xAx            | Data Register A Inputs<br>Data Register B Outputs |
| xBx            | Data Register B Inputs<br>Data Register A Outputs |
| xCLKAB, xCLKBA | Clock Pulse Inputs                                |
| xSAB, xSBA     | Output Data Source Select Inputs                  |
| xDIR, xOE      | Output Enable Inputs                              |

FUNCTION TABLE(1)

| Inputs |      |        |        |      |      | Data I/O <sup>(2)</sup> |        | Operation or Function     |
|--------|------|--------|--------|------|------|-------------------------|--------|---------------------------|
| xOE    | xDIR | xCLKAB | xCLKBA | xSAB | xSBA | xAx                     | xBx    |                           |
| H      | X    | H or L | H or L | X    | X    | Input                   | Input  | Isolation                 |
| H      | X    | ↑      | ↑      | X    | X    |                         |        | Store A and B Data        |
| L      | L    | X      | X      | X    | L    | Output                  | Input  | Real Time B Data to A Bus |
| L      | L    | X      | H or L | X    | H    |                         |        | Stored B Data to A Bus    |
| L      | H    | X      | X      | L    | X    | Input                   | Output | Real Time A Data to B Bus |
| L      | L    | H or L | X      | H    | X    |                         |        | Stored A Data to B Bus    |

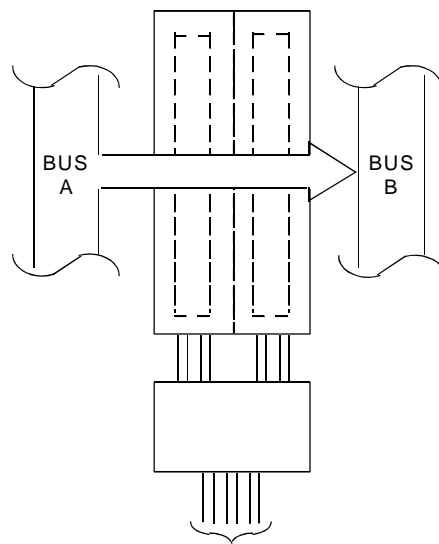
NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance
- The data output functions may be enabled or disabled by various signals at the xOE or xDIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.



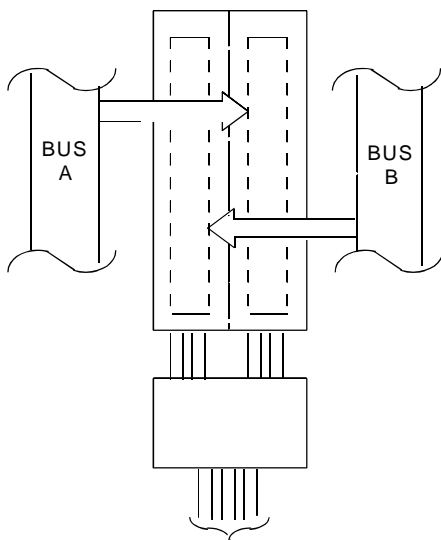
|      |                  |        |        |      |      |
|------|------------------|--------|--------|------|------|
| xDIR | $\overline{xOE}$ | xCLKAB | xCLKBA | xSAB | xSBA |
| L    | L                | X      | X      | X    | L    |

REAL-TIME TRANSFER  
BUS B TO A



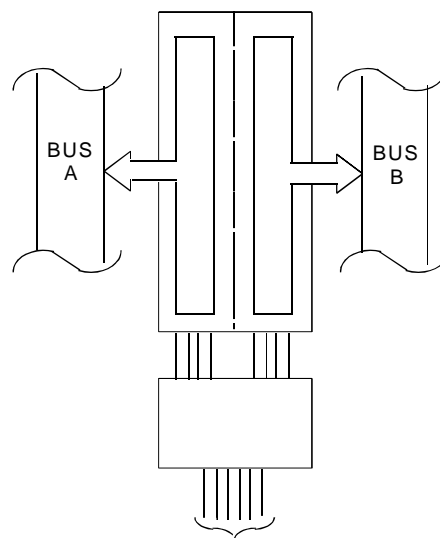
|      |                  |        |        |      |      |
|------|------------------|--------|--------|------|------|
| xDIR | $\overline{xOE}$ | xCLKAB | xCLKBA | xSAB | xSBA |
| H    | L                | X      | X      | L    | X    |

REAL-TIME TRANSFER  
BUS A TO B



|      |                  |        |        |      |      |
|------|------------------|--------|--------|------|------|
| xDIR | $\overline{xOE}$ | xCLKAB | xCLKBA | xSAB | xSBA |
| H    | L                | ↑      | X      | X    | X    |
| L    | L                | X      | ↑      | X    | X    |
| X    | H                | ↑      | ↑      | X    | X    |

STORAGE FROM  
A AND/OR B



|                     |                  |        |        |      |      |
|---------------------|------------------|--------|--------|------|------|
| xDIR <sup>(1)</sup> | $\overline{xOE}$ | xCLKAB | xCLKBA | xSAB | xSBA |
| L                   | L                | X      | H or L | X    | H    |
| H                   | L                | H or L | X      | H    | X    |

TRANSFER STORED  
DATA TO A AND/OR B

NOTE:

1. Cannot transfer data to A bus and B bus simultaneously.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

| Symbol                              | Parameter   | Test Conditions <sup>(1)</sup>                              |                     | Min. | Typ. <sup>(2)</sup> | Max.    | Unit          |
|-------------------------------------|---|---|---------------------|------|---------------------|---------|---------------|
| $V_{IH}$                            | Input HIGH Level  | Guaranteed Logic HIGH Level                                 |                     | 2    | —                   | —       | V             |
| $V_{IL}$                            | Input LOW Level   | Guaranteed Logic LOW Level                                  |                     | —    | —                   | 0.8     | V             |
| $I_{IH}$                            | Input HIGH Current (Input pins) <sup>(5)</sup>                        | $V_{CC} = \text{Max.}$                                      | $V_i = V_{CC}$      | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
|                                     | Input HIGH Current (I/O pins) <sup>(5)</sup>                          |   |                     | —    | —                   | $\pm 1$ |               |
| $I_{IL}$                            | Input LOW Current (Input pins) <sup>(5)</sup>                         |   | $V_i = \text{GND}$  | —    | —                   | $\pm 1$ |               |
|                                     | Input LOW Current (I/O pins) <sup>(5)</sup>                           |   |                     | —    | —                   | $\pm 1$ |               |
| $I_{OZH}$                           | High Impedance Output Current<br>(3-State Output pins) <sup>(5)</sup> | $V_{CC} = \text{Max.}$                                      | $V_o = 2.7\text{V}$ | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
| $I_{OZL}$                           |   |   | $V_o = 0.5\text{V}$ | —    | —                   | $\pm 1$ |               |
| $V_{IK}$                            | Clamp Diode Voltage   | $V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$               |                     | —    | -0.7                | -1.2    | V             |
| $I_{OS}$                            | Short Circuit Current   | $V_{CC} = \text{Max.}, V_o = \text{GND}^{(3)}$              |                     | -80  | -140                | -250    | mA            |
| $V_H$                               | Input Hysteresis  | —   |                     | —    | 100                 | —       | mV            |
| $I_{CCL}$<br>$I_{CCH}$<br>$I_{CCZ}$ | Quiescent Power Supply Current  | $V_{CC} = \text{Max.}$<br>$V_{IN} = \text{GND}$ or $V_{CC}$ |                     | —    | 5                   | 500     | $\mu\text{A}$ |

## OUTPUT DRIVE CHARACTERISTICS

| Symbol    | Parameter                                     | Test Conditions <sup>(1)</sup>                          |                               | Min. | Typ. <sup>(2)</sup> | Max.    | Unit          |
|-----------|---|---|-------------------------------|------|---------------------|---------|---------------|
| $I_o$     | Output Drive Current                          | $V_{CC} = \text{Max.}, V_o = 2.5\text{V}^{(3)}$         |                               | -50  | —                   | -180    | mA            |
| $V_{OH}$  | Output HIGH Voltage                           | $V_{CC} = \text{Min.}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -3\text{mA}$        | 2.5  | 3.5                 | —       | V             |
|           |   |   | $I_{OH} = -15\text{mA}$       | 2.4  | 3.5                 | —       |               |
|           |   |   | $I_{OH} = -32\text{mA}^{(4)}$ | 2    | 3                   | —       |               |
| $V_{OL}$  | Output LOW Voltage                            | $V_{CC} = \text{Min.}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 64\text{mA}$        | —    | 0.2                 | 0.55    | V             |
| $I_{OFF}$ | Input/Output Power Off Leakage <sup>(5)</sup> | $V_{CC} = 0\text{V}, V_{IN}$ or $V_o \leq 4.5\text{V}$  |                               | —    | —                   | $\pm 1$ | $\mu\text{A}$ |

### NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .

## POWER SUPPLY CHARACTERISTICS

| Symbol          | Parameter                                      | Test Conditions <sup>(1)</sup>   | Min.                                       | Typ. <sup>(2)</sup> | Max. | Unit                            |    |
|-----------------|--|--|--|---------------------|------|---------------------------------|----|
| $\Delta I_{CC}$ | Quiescent Power Supply Current TTL Inputs HIGH | $V_{CC} = \text{Max.}$<br>$V_{IN} = 3.4V^{(3)}$  | —  | 0.5                 | 1.5  | mA                              |    |
| $I_{CCD}$       | Dynamic Power Supply Current <sup>(4)</sup>    | $V_{CC} = \text{Max.}$ ,<br>Outputs Open<br>$\overline{xOE} = xDIR = \text{GND}$<br>One Input Toggling<br>50% Duty Cycle   | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —                   | 75   | 120<br>$\mu\text{A}/\text{MHz}$ |    |
| $I_C$           | Total Power Supply Current <sup>(6)</sup>      | $V_{CC} = \text{Max.}$ ,<br>Outputs Open<br>$f_{CP} = 10\text{MHz}$ (xCLKBA)<br>50% Duty Cycle<br>$\overline{xOE} = xDIR = \text{GND}$<br>$f_i = 5\text{MHz}$<br>50% Duty Cycle<br>One Bit Toggling        | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —                   | 0.8  | 1.7                             | mA |
|                 |  |  | $V_{IN} = 3.4V$<br>$V_{IN} = \text{GND}$   | —                   | 1.3  | 3.2                             |    |
|                 |  | $V_{CC} = \text{Max.}$ ,<br>Outputs Open<br>$f_{CP} = 10\text{MHz}$ (xCLKBA)<br>50% Duty Cycle<br>$\overline{xOE} = xDIR = \text{GND}$<br>Sixteen Bits Toggling<br>$f_i = 2.5\text{MHz}$<br>50% Duty Cycle | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —                   | 3.8  | 6.5 <sup>(5)</sup>              |    |
|                 |  |  | $V_{IN} = 3.4V$<br>$V_{IN} = \text{GND}$   | —                   | 8.3  | 20 <sup>(5)</sup>               |    |

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$

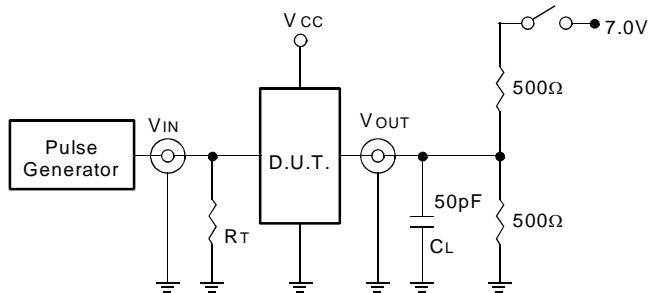
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol                               | Parameter                                 | Condition <sup>(1)</sup> | FCT16646AT          |      | FCT16646CT          |      | FCT16646ET          |      | Unit |
|--------------------------------------|---|--------------------------|---------------------|------|---------------------|------|---------------------|------|------|
|                                      |   |                          | Min. <sup>(2)</sup> | Max. | Min. <sup>(2)</sup> | Max. | Min. <sup>(2)</sup> | Max. |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>Bus to Bus           | CL = 50pF<br>RL = 500Ω   | 2                   | 6.3  | 1.5                 | 5.4  | 1.5                 | 3.8  | ns   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable Time<br>xDIR or xOE to Bus  |                          | 2                   | 9.8  | 1.5                 | 7.8  | 1.5                 | 4.8  | ns   |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable Time<br>xDIR or xOE to Bus |                          | 2                   | 6.3  | 1.5                 | 6.3  | 1.5                 | 4    | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>Clock to Bus         |                          | 2                   | 6.3  | 1.5                 | 5.7  | 1.5                 | 3.8  | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>xSBA or xSAB to Bus  |                          | 2                   | 7.7  | 1.5                 | 6.2  | 1.5                 | 4.2  | ns   |
| t <sub>SU</sub>                      | Set-up Time HIGH or LOW, Bus to Clock     |                          | 2                   | —    | 2                   | —    | 2                   | —    | ns   |
| t <sub>H</sub>                       | Hold Time HIGH or LOW, Bus to Clock       |                          | 1.5                 | —    | 1.5                 | —    | 0                   | —    | ns   |
| t <sub>w</sub>                       | Clock Pulse Width HIGH or LOW             |                          | 5                   | —    | 5                   | —    | 3 <sup>(4)</sup>    | —    | ns   |
| t <sub>sk(0)</sub>                   | Output Skew <sup>(3)</sup>                |                          | —                   | 0.5  | —                   | 0.5  | —                   | 0.5  | ns   |

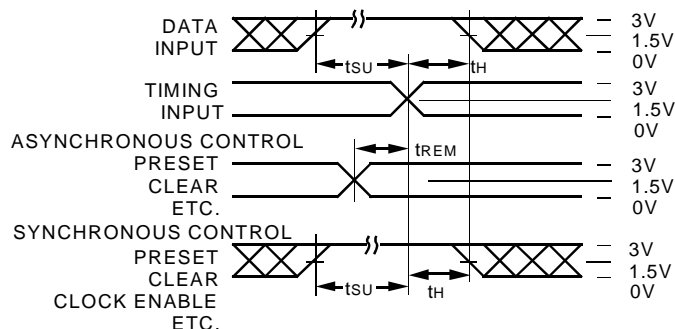
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

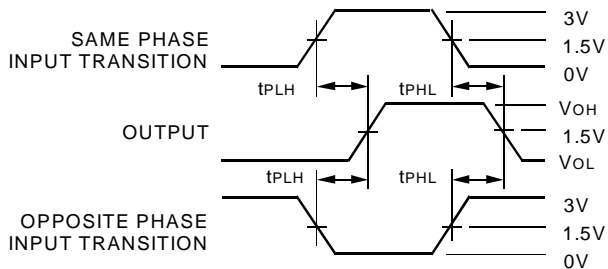
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



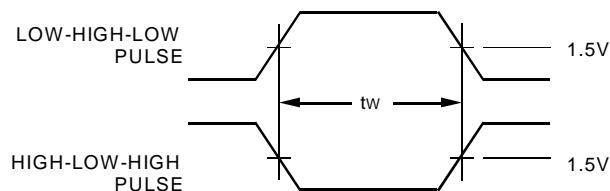
Propagation Delay

SWITCH POSITION

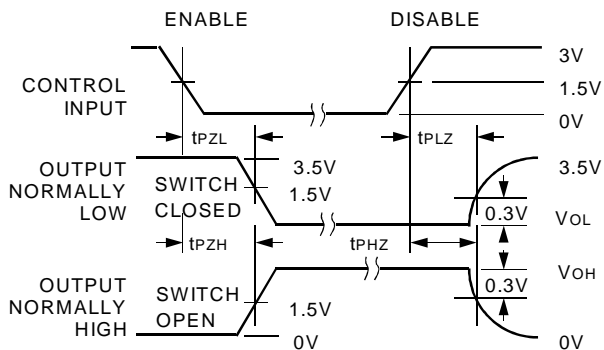
| Test                                    | Switch |
|---|--------|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests                         | Open   |

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to Zout of the Pulse Generator.



Pulse Width

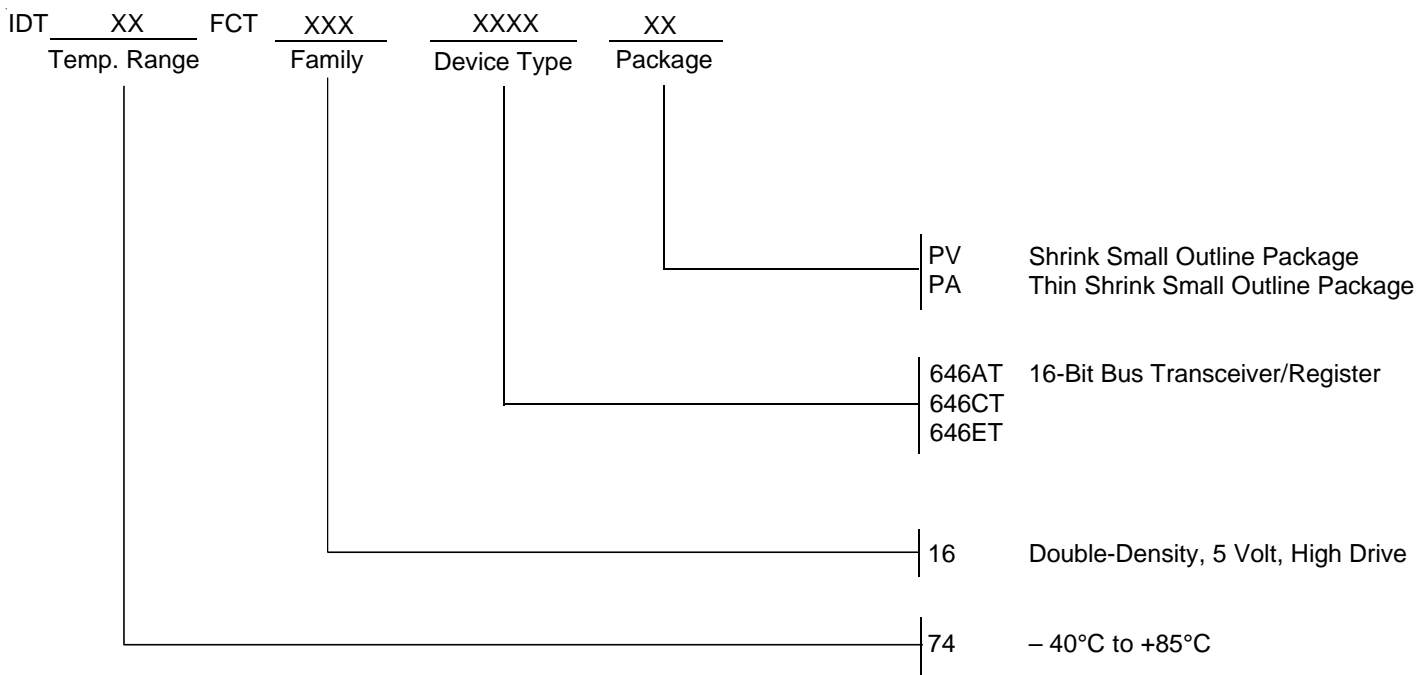


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns.

## ORDERING INFORMATION



## DATA SHEET DOCUMENT HISTORY

- 5/21/2002 Removed TVSOP package
- 6/21/2002 Updated according to PDNs Logic-00-07 and Logic-01-04



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