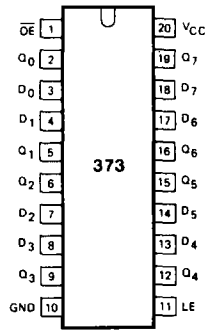
GD54/74HC373, GD54/74HCT373
OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCHES

General Description

These devices are identical in pinout to the 54/74LS374. They contain eight D-type master/slave flip-flops with a common clock and clear. Data meeting the setup and hold time requirements are transferred to the 3-state outputs on the rising edge of the clock pulse. The output enable input does not affect the states of the flip-flops, but when output enable is high, the outputs are forced to the device is not selected. The HC/HCT 373 are identical in function to the HC/HCT 573 which have the input pins on the opposite side of the package from the output pins. They are similar in function to the HC/HCT 533 which have inverting outputs. These devices are characterized for operation over wide temperature rages to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
  for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
enable and read register	L	H	L	L	L
(transparent mode)	L	H	H	H	H
latch and read	L	L	l	L	L
register	L	L	h	H	H
latch register and	H	L	l	L	Z
disable outputs	H	L	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high impedance OFF-state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		−0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC}+0.5V$		|20|	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC}+0.5V$		|35|	mA
I_{CC}	DC V_{CC} or GND current			|70|	mA
T_{stg}	Storage temperature range		−65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC}: GD54/74HC Types	2	6	V
GD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A: GD74 Types	−40	+85	°C
GD54 Types	−55	+125	
Input Rise and Fall times t_r, t_f: GD54/74HC Types at 2V		1000	ns
at 4.5V		500	
at 6V		400	
GD54/74HCT Types at 4.5 V		500	

Logic Diagram

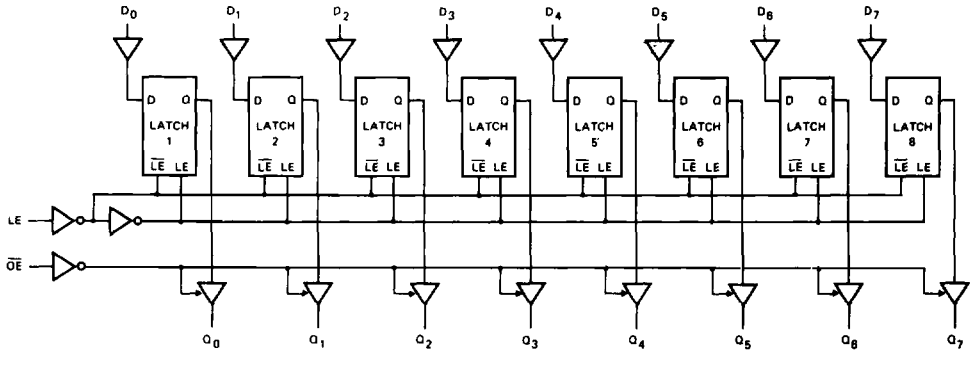


Fig. 1 Logic diagram.

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C			GD74HC373		GD54HC373		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage			2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V_{IL}	LOW level input voltage			2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
			$I_{OH}=-6mA$ $I_{OH}=-7.8mA$	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
			$I_{OL}=6mA$ $I_{OL}=7.8mA$	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
$\|I_{IN}\|$	Input leakage Current	$V_{IN}=V_{CC}$ or GND		6.0			0.1		1.0		1.0	μA
I_{OZ}	Three-State leakage current	$V_{IN}=V_{IH}$ or V_{IL}	$V_O=V_{CC}$ or GND	6.0		0.01	0.5		5.0		10.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu A$		6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C			GD74HCT373		GD54HCT373		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage			4.5 to 5.0	2.0			2.0		2.0		V
V_{IL}	LOW level input voltage			4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	4.5	4.4	4.5		4.4		4.4		V
			$I_{OH}=-6mA$	4.5	3.98	4.3		3.84		3.7		
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	4.5			0.1		0.1		0.1	V
			$I_{OL}=6mA$	4.5		0.17	0.26		0.33		0.4	
$\|I_{IN}\|$	Input leakage Current	$V_{IN}=V_{CC}$ or GND		5.5			0.1		1.0		1.0	μA
I_{OZ}	Three-State leakage current	$V_{IN}=V_{IH}$ or V_{IL}	$V_O=V_{CC}$ or GND	5.5		0.01	0.5		5.0		10.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu A$		5.5			8		80		160	μA

Timing Requirement for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25°C$			GD74HC373		GD54HC373		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	LE high	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Setup time	Data before LE ↓	2.0	60	30		100		120		ns
			4.5	12	10		20		25		
			6.0	10	8		18		22		
t_h	Hold time	Data after LE ↓	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25°C$			GD74HC373		GD54HC373		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH}/ t_{PHL}	Propagation Delay Time Dn to Qn	2.0		40	140		180		210	ns
		4.5		14	28		36		40	
		6.0		12	26		33		38	
t_{PLH}/ t_{PHL}	Propagation Delay Time LE to Qn	2.0		42	150		190		220	ns
		4.5		16	32		42		50	
		6.0		14	30		38		45	
t_{PZH}/ t_{PZL}	3-state Output Enable Time $\overline{OE}$ to Q_n	2.0		45	150		190		220	ns
		4.5		15	30		38		45	
		6.0		14	26		33		38	
t_{PLZ}/ t_{PHZ}	3-state Output Disable Time $\overline{OE}$ to Q_n	2.0		45	150		190		220	ns
		4.5		15	30		38		45	
		6.0		14	26		33		38	
t_{TLH}/ t_{THL}	Output Transition Time	2.0		15	60		75		90	ns
		4.5		6	12		15		18	
		6.0		5	10		13		15	

Timing Requirements for HCT: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25°C$			GD74HCT373		GD54HCT373		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	LE high	4.5	16	10		20		25		ns
t_{su}	Setup time	Data after LE ↓	4.5	12	10		20		25		ns
t_h	Hold time	Data before LE ↓	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25°C$			GD74HCT373		GD54HCT373		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Time D_n to Q_n	4.5		16	30		38		44	ns
t_{PLH}/ t_{PHL}	Propagation Delay Time LE to Q_n	4.5		19	35		42		48	ns
t_{PZH}/ t_{PZL}	3-state Output Enable time $\overline{OE}$ to Q_n	4.5		15	30		38		45	ns
t_{PLZ} t_{PHZ}	3-state Output Disable Time $\overline{OE}$ to Q_n	4.5		15	30		38		45	ns
t_{TLH}/ t_{THL}	Output Transition Time	4.5		6	12		15		18	ns

AC Waveforms

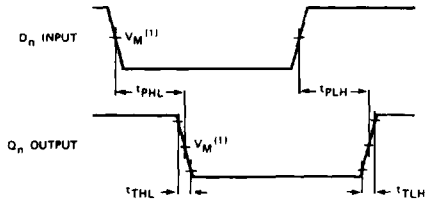


Fig. 2 Waveforms showing the data input (D_n) to output (Q_n) propagation delays and the output transition times.

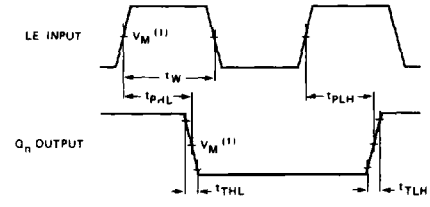


Fig. 3 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.

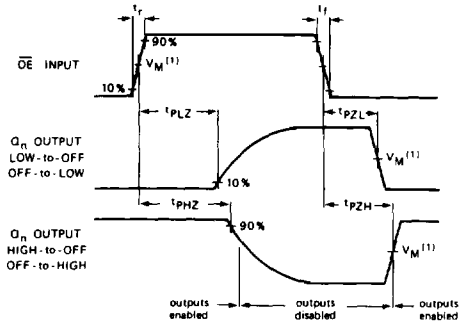


Fig. 4 Waveforms showing the 3-state enable and disable time.

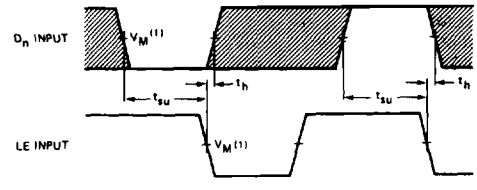


Fig. 5 Waveforms showing the data set-up and hold times for D_n input to LE input.

Note to Fig. 5

The shaded areas indicate when the input is permitted to change for predicable output performance.

Note to AC waveforms

(1) HC : V_M=50%; V_I=GND to V_{CC}.
HCT: V_M=1.3V; V_I=GND to 3V.