DATA SHEET

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- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4013B
flip-flops
Dual D-type flip-flop

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

Dual D-type flip-flop

HEF4013B flip-flops

DESCRIPTION

The HEF4013B is a dual D-type flip-flop which features independent set direct (S_D), clear direct (C_D), clock inputs (CP) and outputs (O, $\overline{O}$). Data is accepted when CP is LOW and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and override the D or CP inputs. The outputs are buffered for best system performance. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

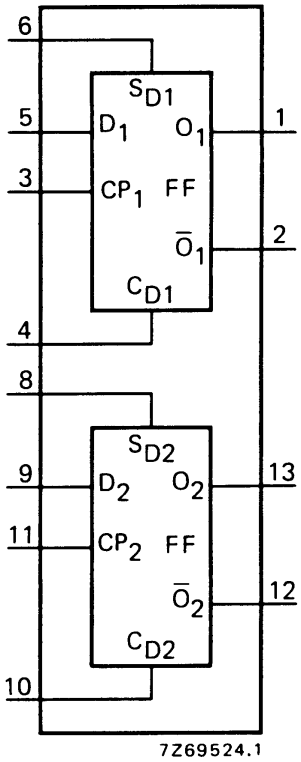

Fig.1 Functional diagram.

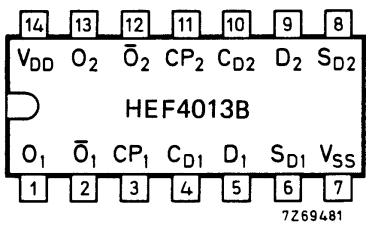

Fig.2 Pinning diagram.

FUNCTION TABLES

INPUTS				OUTPUTS	
S_D	C_D	CP	D	O	$\overline{O}$
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H

INPUTS				OUTPUTS	
S_D	C_D	CP	D	$O_n + 1$	$\overline{O}_n + 1$
L	L	⟋	L	L	H
L	L	⟋	H	H	L

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   ⟋ = positive-going transition
   $O_n + 1$ = state after clock positive transition

PINNING

D	data inputs
CP	clock input (L to H edge-triggered)
S_D	asynchronous set-direct input (active HIGH)
C_D	asynchronous clear-direct input (active HIGH)
O	true output
$\overline{O}$	complement output

HEF4013BP(N):	14-lead DIL; plastic (SOT27-1)
HEF4013BD(F):	14-lead DIL; ceramic (cerdip) (SOT73)
HEF4013BT(D):	14-lead SO; plastic (SOT108-1)

( ): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category FLIP-FLOPS

See Family Specifications

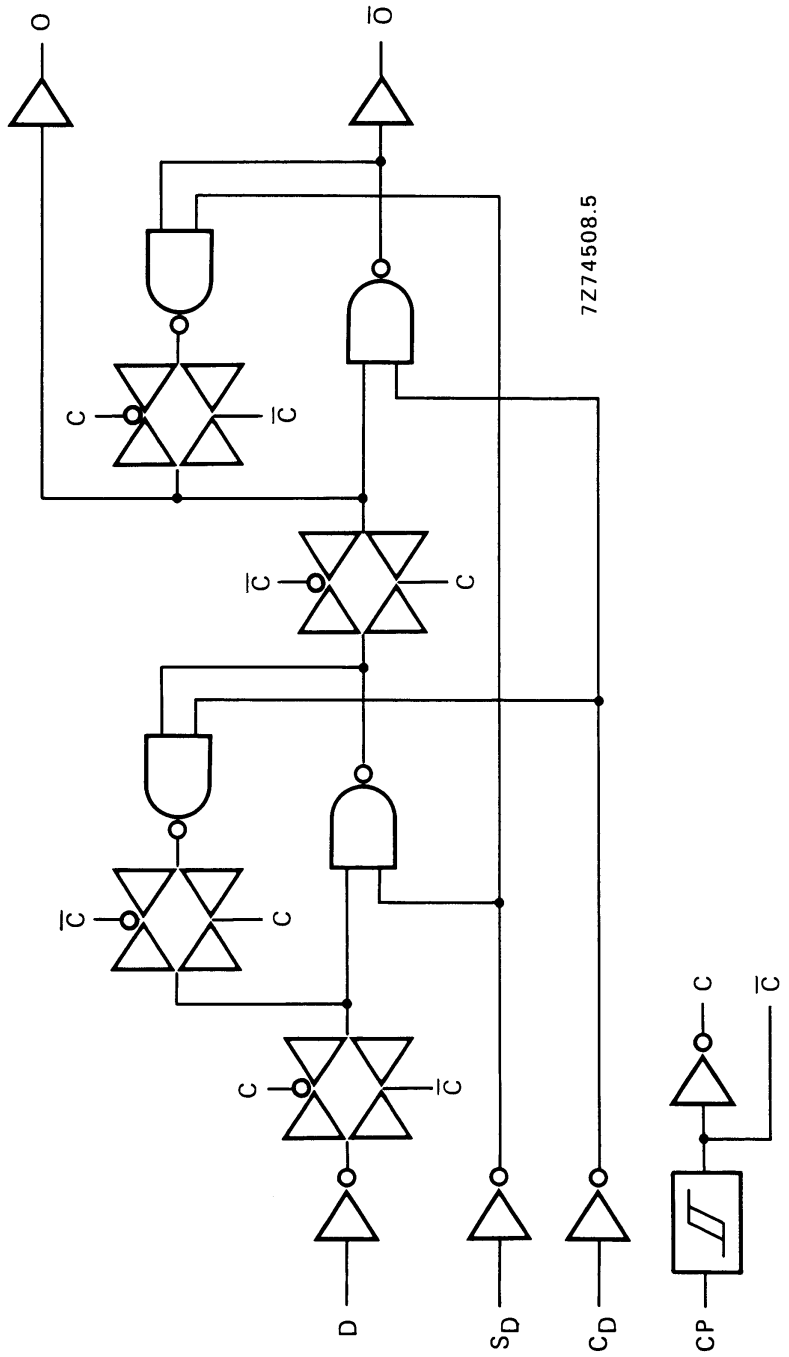

Fig.3 Logic diagram (one flip-flop).

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
CP → O, $\overline{O}$	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
S_D → $\overline{O}$	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
S_D → O	5			75	150	ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
C_D → O	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
C_D → $\overline{O}$	5			60	120	ns	33 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			20	40	ns	12 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

AC CHARACTERISTI CS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	
Set-up time	5		40	20	ns	see also waveforms Figs 4 and 5
D → CP	10	t_{su}	25	10	ns	
	15		15	5	ns	
Hold time	5		20	0	ns	
D → CP	10	t_{hold}	20	0	ns	
	15		15	0	ns	
Minimum clock	5		60	30	ns	
pulse width; LOW	10	t_{WCPL}	30	15	ns	
	15		20	10	ns	
Minimum S_D pulse	5		50	25	ns	
width; HIGH	10	t_{WSDH}	24	12	ns	
	15		20	10	ns	
Minimum C_D pulse	5		50	25	ns	
width; HIGH	10	t_{WCDH}	24	12	ns	
	15		20	10	ns	
Recovery time	5		15	–5	ns	
for S_D	10	t_{RSD}	15	0	ns	
	15		15	0	ns	
Recovery time	5		40	25	ns	
for C_D	10	t_{RCD}	25	10	ns	
	15		25	10	ns	
Maximum clock	5		7	14	MHz	
pulse frequency	10	f_{max}	14	28	MHz	
	15		20	40	MHz	

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	$850\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where
dissipation per	10	$3\ 600\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
package (P)	15	$9\ 000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = total load cap. (pF)
			$\sum (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

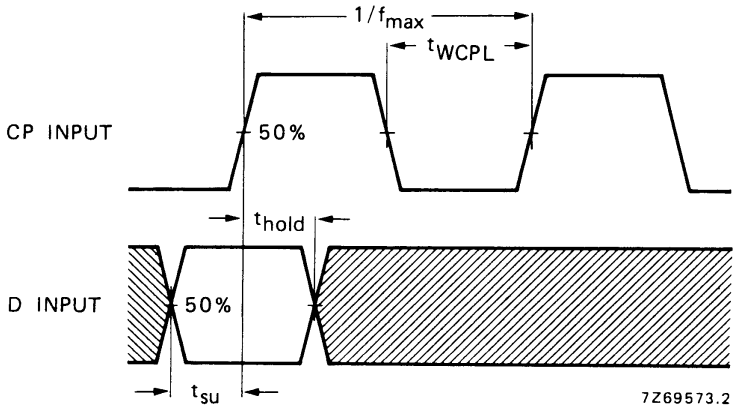

Fig.4 Waveforms showing set-up times, hold times and minimum clock pulse width. Set-up and hold times are shown as positive values but may be specified as negative values.

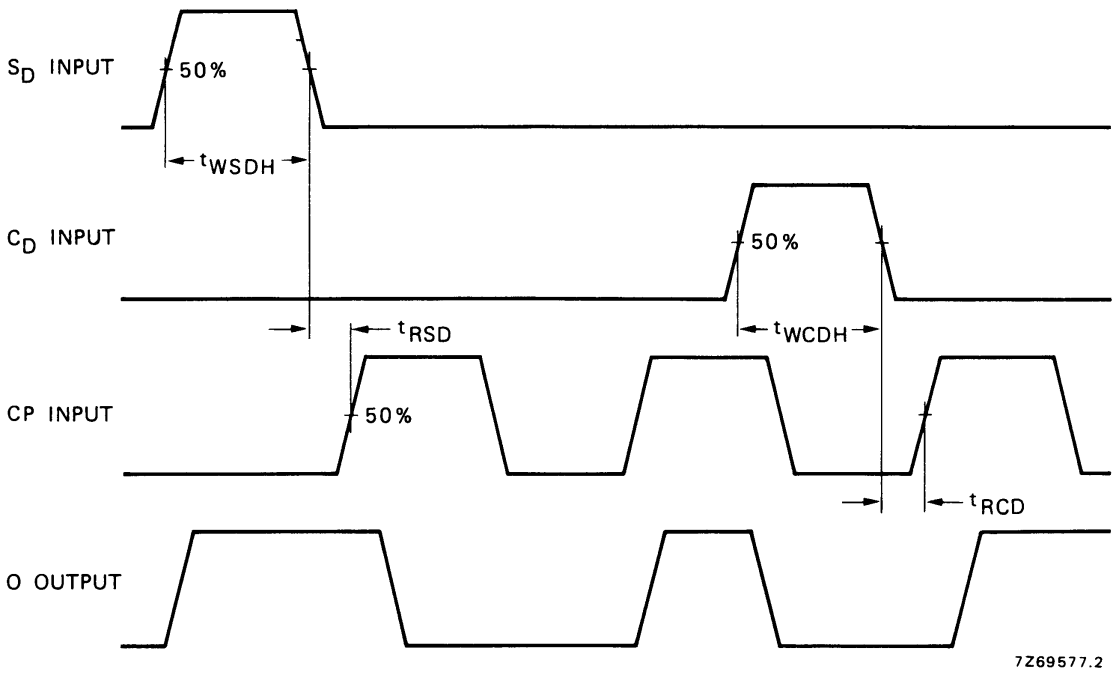

Fig.5 Waveforms showing recovery times for S_D and C_D; minimum S_D and C_D pulse widths.

APPLICATION INFORMATION

Some examples of applications for the HEF4013B are:

- Counters/dividers
- Registers
- Toggle flip-flops

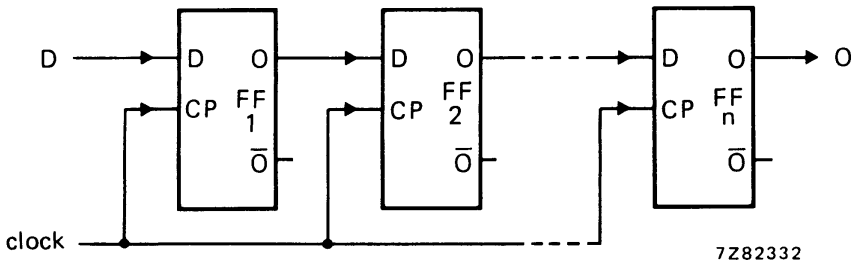

Fig.6 Typical application of the HEF4013B in an n-stage shift register.

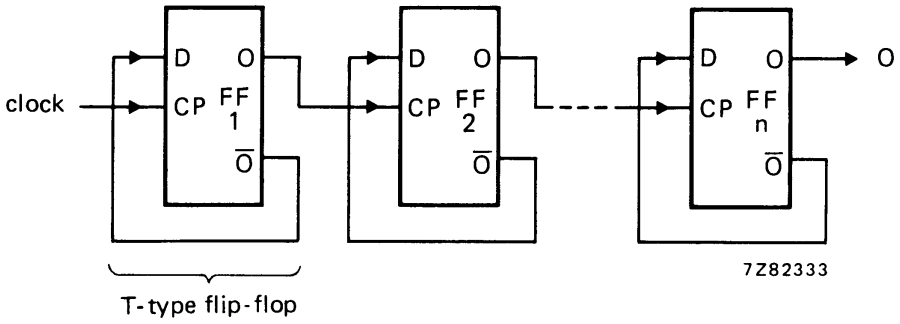

Fig.7 Typical application of the HEF4013B in a binary ripple up-counter; divide-by-2^n.

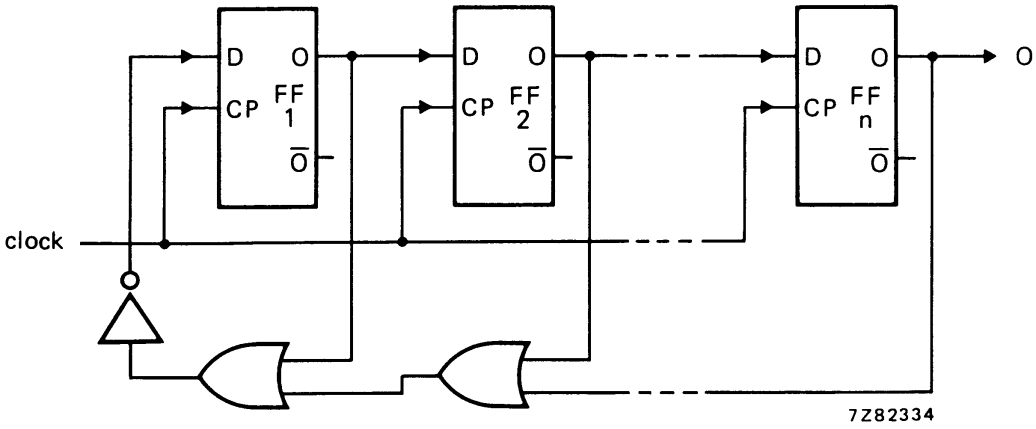

Fig.8 Typical application of the HEF4013B in a modified ring counter; divide-by-(n + 1).

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Information as of 2000-08-29

HEF4013B; Dual D-type flip-flop

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Description

The HEF4013B is a dual D-type flip-flop which features independent set direct (S_D), clear direct (C_D), clock inputs (CP) and outputs (O, O). Data is accepted when CP is LOW and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and override the D or CP inputs. The outputs are buffered for best system performance. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

Datasheet

Type nr.	Title	Publication release date	Datasheet status	Page count	File size (kB)	Datasheet
HEF4013B	Dual D-type flip-flop	01-Jan-95	Product Specification	7	79	Download

Additional datasheet info

To complete the device datasheet with package and family information, also download the following PDF files .

	Document	Description	Refer to catalog
1	HEF_FAMILY_SPECIFICATIONS	HEF Family Specifications, The IC04 LOCMOS HE4000B Logic	ICL02

Family Specifications HEF, HEC

2	HEF_PACKAGE_OUTLINES	HEF Package Outlines/Info, The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC	ICL02

Products, packages, availability and ordering

Partnumber	North American Partnumber	Order code (12nc)	marking/packing	package	device status	buy online
HEC4013BT		9352 298 80112	Standard Marking * Bulk Pack	SOT108	Full production	-
		9352 298 80118	Standard Marking * Reel Pack, SMD, 13"	SOT108	Full production	-
HEF4013BP	HEF4013BPN	9332 776 10652	Standard Marking * Bulk Pack, CECC	SOT27	Full production	
HEF4013BT	HEF4013BTD	9333 726 60652	Standard Marking * Bulk Pack, CECC	SOT108	Full production	
	HEF4013BTD-T	9333 726 60653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT108	Full production	
HEF4013BTS	HEF4013BTSDB	9352 452 90112	Standard Marking * Bulk Pack	SOT337	Full production	
	HEF4013BTSDB-T	9352 452 90118	Standard Marking * Reel Pack, SMD, 13"	SOT337	Full production	
HEF4013BU		9333 736 00005	No Marking * Chips on Wafer, Pre-Sawn, On FFC	NONE	Full production	-

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