

74LCXH162373

Low Voltage 16-Bit Transparent Latch with Bushold and 26Ω Series Resistor Outputs

General Description

The LCXH162373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH, the outputs are in a high impedance state.

The LCXH162373 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The 26Ω series resistor helps reduce output overshoot and undershoot.

The LCXH162373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

The LCXH162373 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

Features

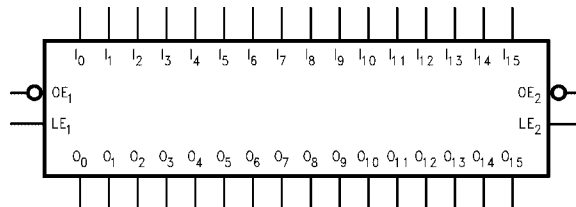
- 5V tolerant control inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- Equivalent 26Ω series resistors on outputs
- Bushold on inputs eliminates the need for external pull-up/pull-down resistors
- 6.2 ns t_{PD} max ($V_{CC} = 3.3V$), 20 μA I_{CC} max
- Power down high impedance inputs and outputs
- ± 12 mA output drive ($V_{CC} = 3.0V$)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

Ordering Code:

Order Number	Package Number	Package Description
74LCXH162373GX (Note 1)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74LCXH162373MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [RAIL]
74LCXH162373MEX	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TAPE and REEL]
74LCXH162373MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [RAIL]
74LCXH162373MTX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

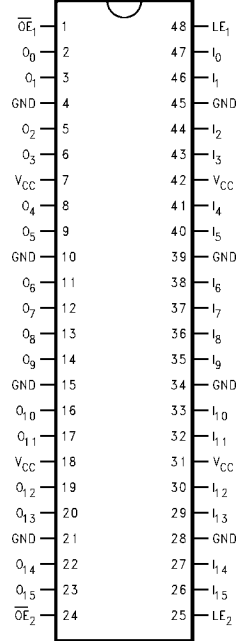
Note 1: BGA package available in Tape and Reel only.

Logic Symbol

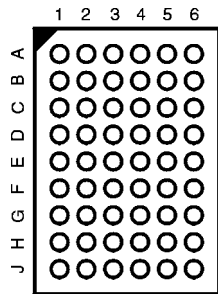


Connection Diagrams

Pin Assignment for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
LE_n	Latch Enable Input
I_0-I_{15}	Inputs (Bushold)
O_0-O_{15}	Outputs (Bushold)
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_0	NC	\overline{OE}_1	LE_1	NC	I_0
B	O_2	O_1	NC	NC	I_1	I_2
C	O_4	O_3	V_{CC}	V_{CC}	I_3	I_4
D	O_6	O_5	GND	GND	I_5	I_6
E	O_8	O_7	GND	GND	I_7	I_8
F	O_{10}	O_9	GND	GND	I_9	I_{10}
G	O_{12}	O_{11}	V_{CC}	V_{CC}	I_{11}	I_{12}
H	O_{14}	O_{13}	NC	NC	I_{13}	I_{14}
J	O_{15}	NC	\overline{OE}_2	LE_2	NC	I_{15}

Truth Tables

Inputs			Outputs
LE_1	\overline{OE}_1	I_0-I_7	O_0-O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

Inputs			Outputs
LE_2	\overline{OE}_2	I_8-I_{15}	O_8-O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

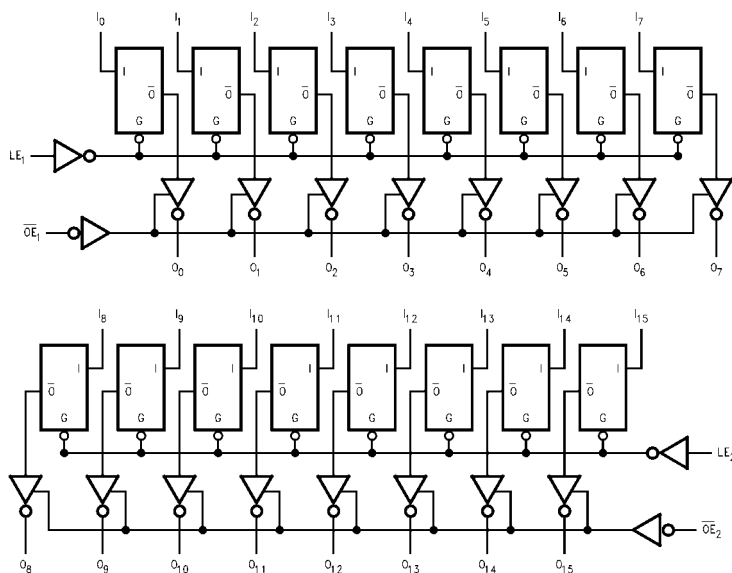
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Functional Description

The LCXH162373 contains sixteen D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the I_n enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each

time its I input changes. When LE_n is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition of LE_n . The 3-STATE standard outputs are controlled by the Output Enable (\overline{OE}_n) input. When \overline{OE}_n is LOW, the standard outputs are in the 2-state mode. When \overline{OE}_n is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)						
Symbol	Parameter	Value	Conditions	Units		
V _{CC}	Supply Voltage	-0.5 to +7.0		V		
V _I	DC Input Voltage	$I_0 - I_{15}$ \overline{OE}_n, LE_n	-0.5 to V _{CC} + 0.5 -0.5V to 7.0V	V		
V _O	DC Output Voltage	-0.5 to +7.0 -0.5 to V _{CC} + 0.5	Output in 3-STATE Output in HIGH or LOW State (Note 3)	V		
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA		
I _{OK}	DC Output Diode Current	-50 +50	V _O < GND V _O > V _{CC}	mA		
I _O	DC Output Source/Sink Current	±50		mA		
I _{CC}	DC Supply Current per Supply Pin	±100		mA		
I _{GND}	DC Ground Current per Ground Pin	±100		mA		
T _{STG}	Storage Temperature	-65 to +150		°C		
Recommended Operating Conditions (Note 4)						
Symbol	Parameter	Min	Max	Units		
V _{CC}	Supply Voltage	Operating	2.0	3.6	V	
		Data Retention	1.5	3.6		
V _I	Input Voltage	0	V _{CC}	V		
V _O	Output Voltage	HIGH or LOW State	0	V _{CC}	V	
		3-STATE	0	5.5		
I _{OH} /I _{OL}	Output Current	V _{CC} = 3.0V – 3.6V		±12	mA	
		V _{CC} = 2.7V – 3.0V		±8		
		V _{CC} = 2.3V – 2.7V		±4		
T _A	Free-Air Operating Temperature	-40	85	°C		
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V	0	10	ns/V		
<p>Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.</p> <p>Note 3: I_O Absolute Maximum Rating must be observed.</p> <p>Note 4: Floating or unused control inputs must be HIGH or LOW.</p>						
DC Electrical Characteristics						
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units
				Min	Max	
V _{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V _{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100 μA	2.3 – 3.6	V _{CC} - 0.2		V
		I _{OH} = -4 mA	2.3	1.8		
		I _{OH} = -4 mA	2.7	2.2		
		I _{OH} = -6 mA	3.0	2.4		
		I _{OH} = -8 mA	2.7	2.0		
		I _{OH} = -12 mA	3.0	2.0		
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3 – 3.6		0.2	V
		I _{OL} = 4 mA	2.3		0.6	
		I _{OL} = 4 mA	2.7		0.4	
		I _{OL} = 6 mA	3.0		0.55	
		I _{OL} = 8 mA	2.7		0.6	
		I _{OL} = 12 mA	3.0		0.8	
I _I	Input Leakage Current	V _I = V _{CC} or GND	2.3 – 3.6		±5.0	μA

DC Electrical Characteristics (Continued)								
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units		
				Min	Max			
I _{I(HOLD)}	Bushold Input Minimum Drive Hold Current	V _{IN} = 0.7V	2.3	45		μA		
		V _{IN} = 1.7V		-45				
		V _{IN} = 0.8V	3.0	75				
		V _{IN} = 2.0V		-75				
I _{I(OD)}	Bushold Input Over-Drive Current to Change State	(Note 6)	2.7	300		μA		
		(Note 7)		-300				
		(Note 6)	3.6	450				
		(Note 7)		-450				
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 5.5V V _I = V _{IH} or V _{IL}	2.3 – 3.6		±5.0	μA		
I _{OFF}	Power-Off Leakage Current	V _O = V _{CC}	0		10	μA		
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.3 – 3.6		20	μA		
		3.6V ≤ V _O ≤ 5.5V (Note 5)	2.3 – 3.6		±20			
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.3 – 3.6		500	μA		
<p>Note 5: Outputs disabled or 3-STATE only.</p> <p>Note 6: An external driver must source at least the specified current to switch from LOW-to-HIGH.</p> <p>Note 7: An external driver must sink at least the specified current to switch from HIGH-to-LOW.</p>								
AC Electrical Characteristics								
Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		
		C _L = 50 pF		C _L = 50 pF		C _L = 30 pF		
		Min	Max	Min	Max	Min	Max	
t _{PHL}	Propagation Delay	1.5	6.2	1.5	6.7	1.5	7.4	ns
t _{PLH}	I _n to O _n	1.5	6.2	1.5	6.7	1.5	7.4	
t _{PHL}	Propagation Delay	1.5	6.3	1.5	7.2	1.5	7.6	ns
t _{PLH}	LE to O _n	1.5	6.3	1.5	7.2	1.5	7.6	
t _{PZL}	Output Enable Time	1.5	6.9	1.5	7.3	1.5	9.0	ns
t _{PZH}		1.5	6.9	1.5	7.3	1.5	9.0	
t _{PLZ}	Output Disable Time	1.5	6.0	1.5	6.3	1.5	7.2	ns
t _{PHZ}		1.5	6.0	1.5	6.3	1.5	7.2	
t _S	Setup Time, I _n to LE	2.5		2.5		3.0		ns
t _H	Hold Time, I _n to LE	1.5		1.5		2.0		ns
t _W	LE Pulse Width	3.0		3.0		3.5		ns
t _{OSSL}	Output to Output Skew (Note 8)		1.0					ns
t _{OSLH}			1.0					
<p>Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.</p>								

Dynamic Switching Characteristics					
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.35	V
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	0.25	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	-0.35	V
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	-0.25	
Capacitance					
Symbol	Parameter	Conditions	Typical	Units	
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	7	pF	
C _{OUT}	Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8	pF	
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC} , f = 10 MHz	20	pF	

AC LOADING and WAVEFORMS Generic for LCX Family

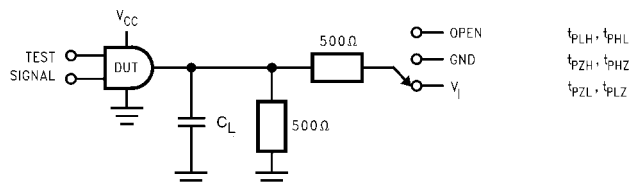
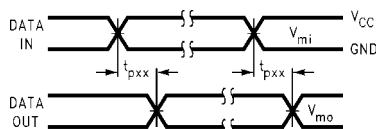
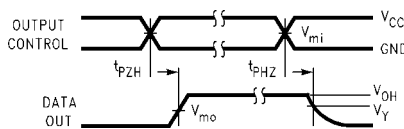


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

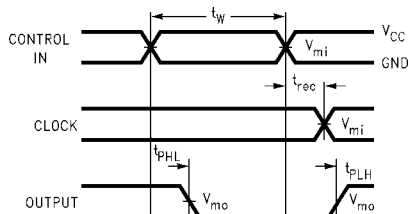
Test	Switch
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$, and 2.7V $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH} , t_{PHZ}	GND



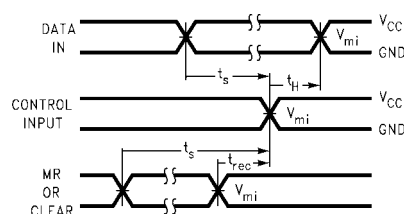
Waveform for Inverting and Non-Inverting Functions



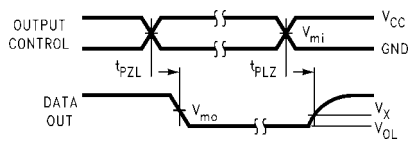
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay, Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

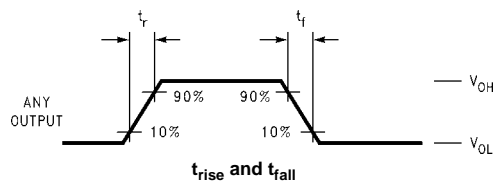
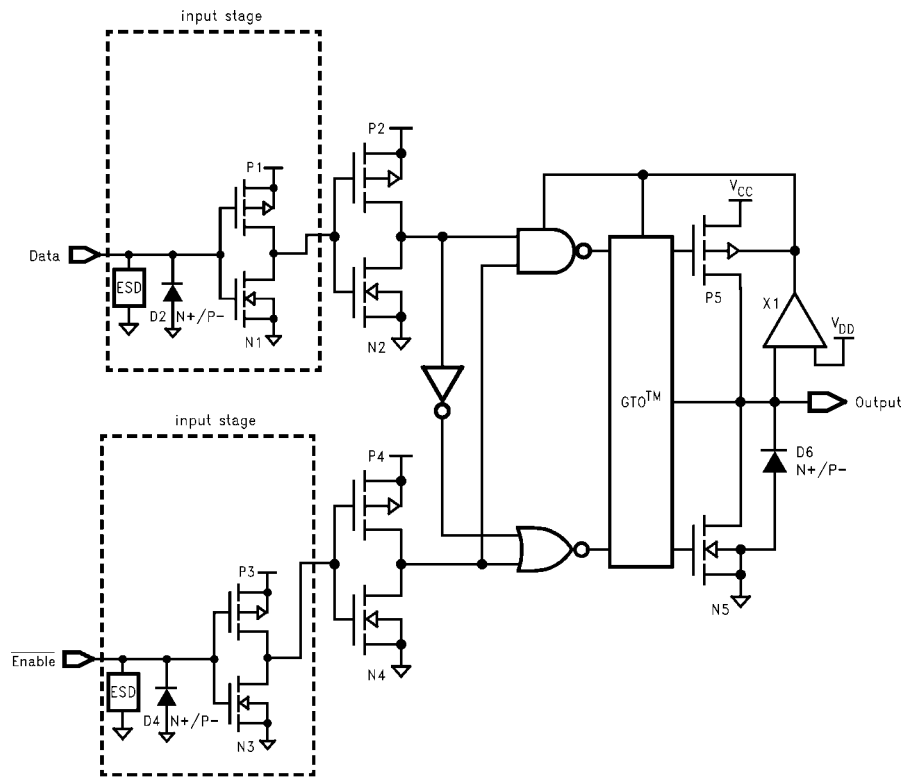


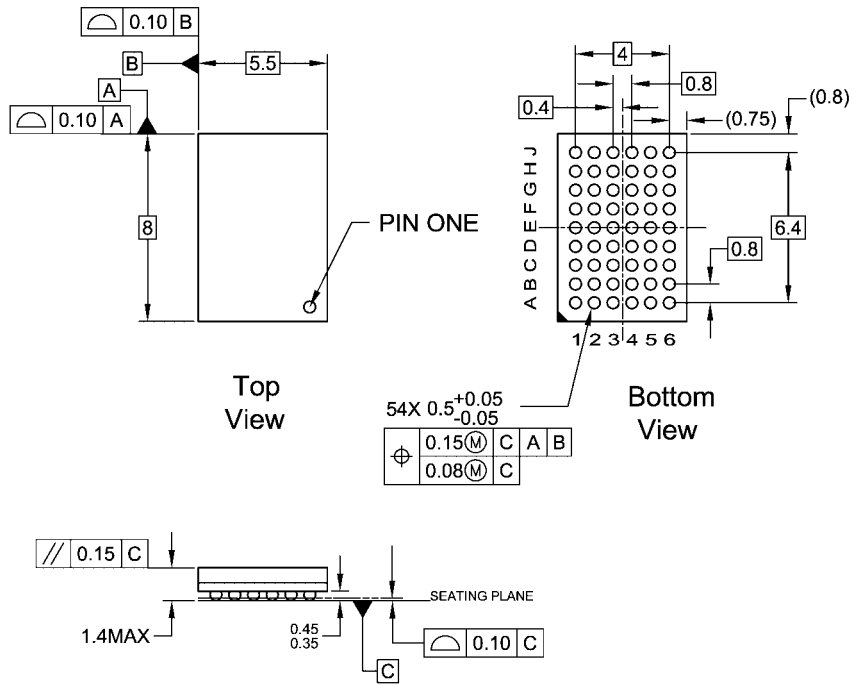
FIGURE 2. Waveforms
(Input Characteristics; $f = 1 \text{ MHz}$, $t_r = t_f = 3 \text{ ns}$)

Symbol	V_{CC}		
	$3.3 \pm 0.3V$	2.7V	$2.5 \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram Generic for LCX Family



Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

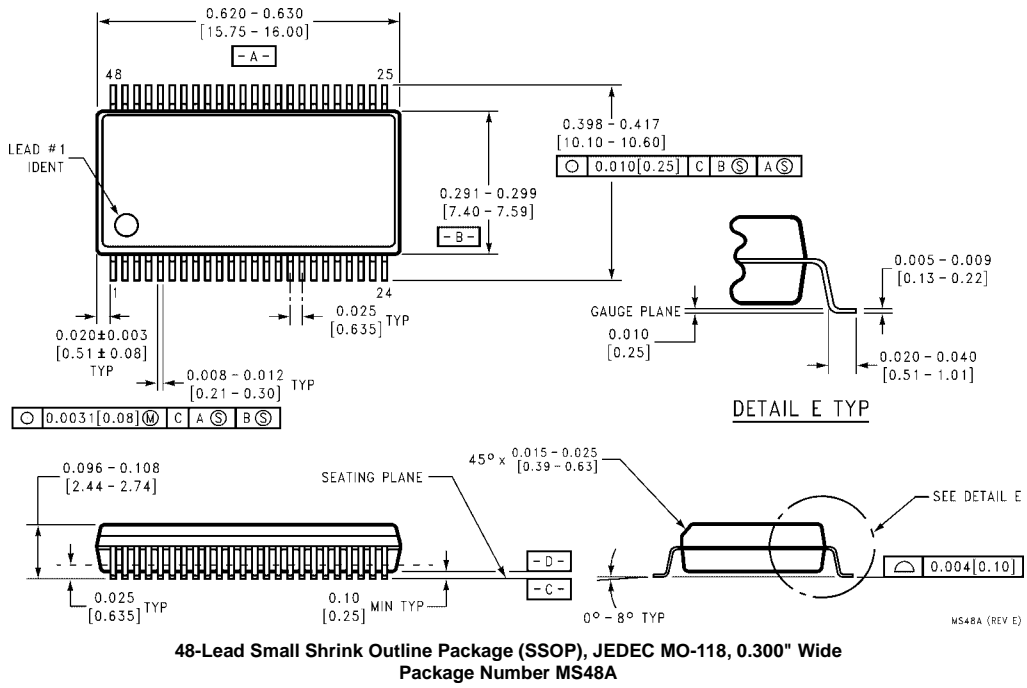
- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

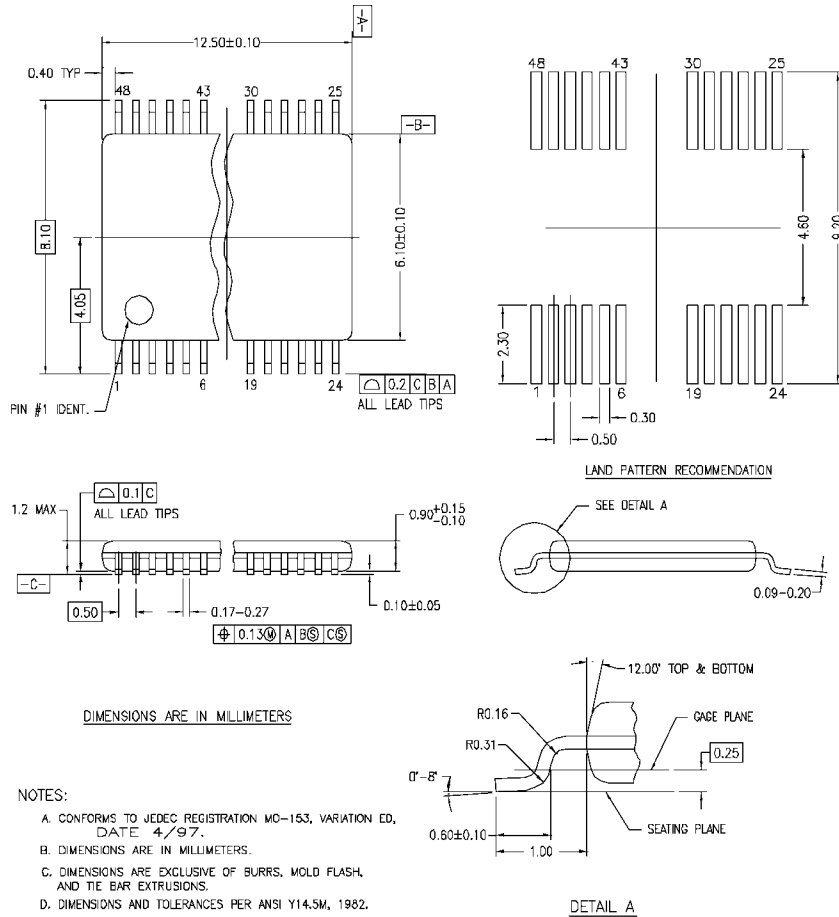
**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC M0-205, 5.5mm Wide
Package Number BGA54A
Preliminary**

74LCXH162373

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com