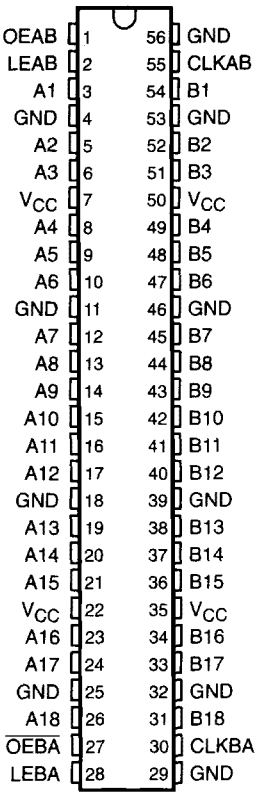
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT16501 . . . WD PACKAGE
SN74LVT16501 . . . DGG OR DL PACKAGE
(TOP VIEW)



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description

The 'LVT16501 is an 18-bit universal bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and $\overline{\text{OEBA}}$ is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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description (continued)

The SN74LVT16501 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16501 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT16501 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

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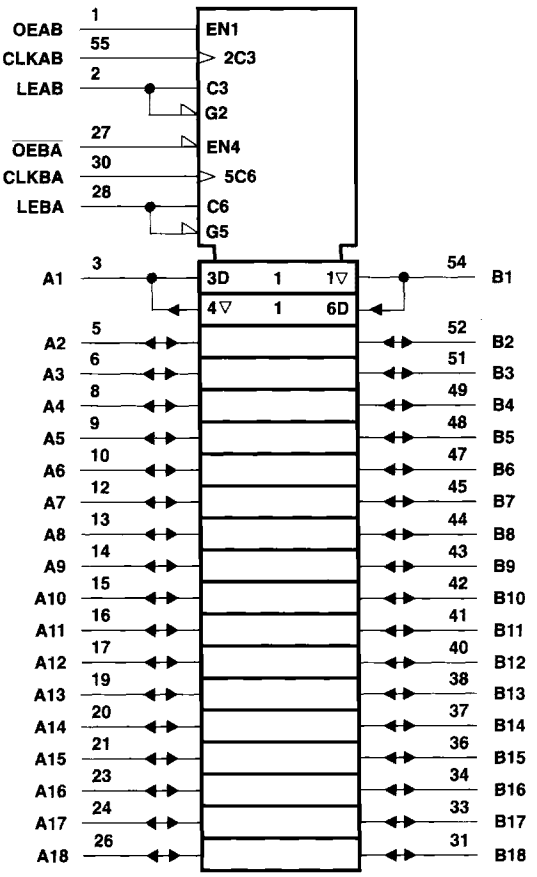
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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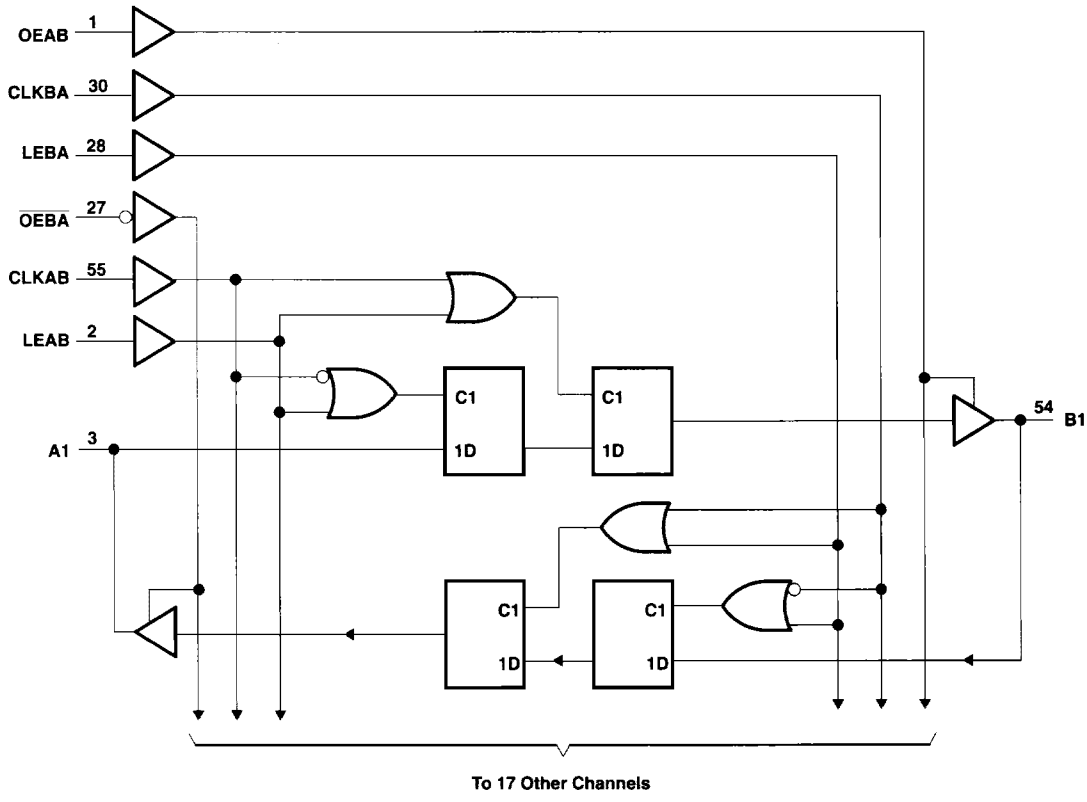
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16501 ..... 96 mA
SN74LVT16501 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16501 ..... 48 mA
SN74LVT16501 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT16501		SN74LVT16501		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}†	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16501		SN74LVT16501		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2		V_{CC}–0.2		V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4		2.4		
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2				
	V_{CC} = 3 V,	I_{OH} = –32 mA				2		
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA			0.2		0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA			0.4		0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA			0.55			
	V_{CC} = 3 V,	I_{OL} = 64 mA					0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§		20		20	
	V_{CC} = 3.6 V,	V_I = V_{CC}			1		1	
	V_{CC} = 3.6 V,	V_I = 0			–5		–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75		75		µA
		V_I = 2 V		–75		–75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–1		–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.1		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.1		0.1	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_{io}	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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