

KS54HCTLS 125/126
KS74HCTLS

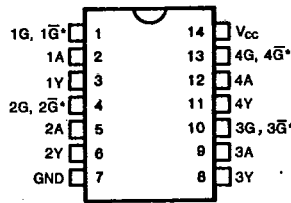
Quad 3-State Buffers

7-5207

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74HCTLS: -40°C to +85°C
 KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION



* \bar{G} for '125; G for '126

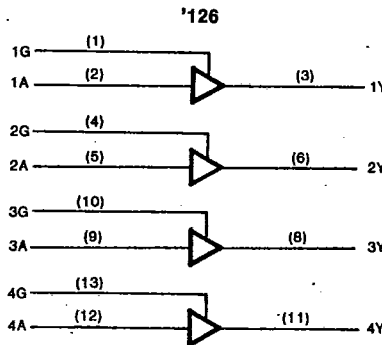
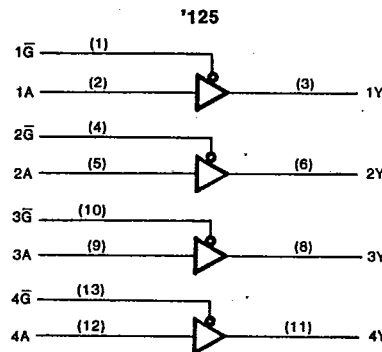
DESCRIPTION

These bus buffers feature four independent line drivers with 3-state outputs. The output enable functions for the '125 buffers are active-low, while those for '126 are active high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{cc} and ground.

LOGIC DIAGRAMS



FUNCTION TABLES

'125

Inputs		Output
A	\bar{G}	Y
H	L	H
L	L	L
X	H	Z

'126

Inputs		Output
A	G	Y
H	H	H
L	H	L
X	L	Z

KS54HCTLS 125/126
KS74HCTLS

Quad 3-State Buffers

T-52-07

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} -0.5V to +7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 70 mA
 Continuous Current Through
 V_{CC} or GND pins ± 250 mA
 Storage Temperature Range, T_{stg} ... -65°C to +150°C
 Power Dissipation Per Package, P_d † 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
 Plastic Package (N): -12mW/°C from 65°C to 85°C
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN}, V_{OUT} ... 0V to V_{CC}
 Operating Temperature
 Range KS74HCTLS: -40°C to +85°C
 KS54HCTLS: -55°C to +125°C
 Input Rise & Fall Times, t_r, t_f Max 500 ns
 * Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$				Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O = -20\mu A$ $I_O = -6mA$	V_{CC} 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable = V_{IH} $V_{OUT}=V_{CC}$ or GND		± 0.5	± 5.0	± 10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I = 2.4V$ other inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

KS54HCTL5 **125/126**
KS74HCTL5

Quad 3-State Buffers

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AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTL5125, HCTL5126

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTL5	KS54HCTL5	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ		Guaranteed Limits		
Maximum Propagation Delay, A to Y	t_{PLH}	$C_L = 50\text{pF}$	13	18	22	27	ns
		$C_L = 150\text{pF}$	16	21	27	33	
	t_{PHL}	$C_L = 50\text{pF}$	13	18	22	27	
		$C_L = 150\text{pF}$	16	21	27	33	
Maximum Output Enable Time, Enable to Y	t_{PZH}	$C_L = 50\text{pF}$	17	23	29	34	ns
		$C_L = 150\text{pF}$	20	26	34	40	
	t_{PZL}	$C_L = 50\text{pF}$	17	23	29	34	
		$C_L = 150\text{pF}$	20	26	34	40	
Maximum Output Disable Time, Enable to Y	t_{PHZ}	$R_L = 1\text{k}\Omega$	16		26	32	ns
	t_{PLZ}	$C_L = 50\text{pF}$	16		26	32	
Maximum Input Capacitance	C_{IN}		5				pF
Maximum Output Capacitance	C_{OUT}	Output Disabled	10				pF
Power Dissipation Capacitance* (per stage)	C_{PD}	Output Disabled	5				pF
		Output Enabled	30				

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

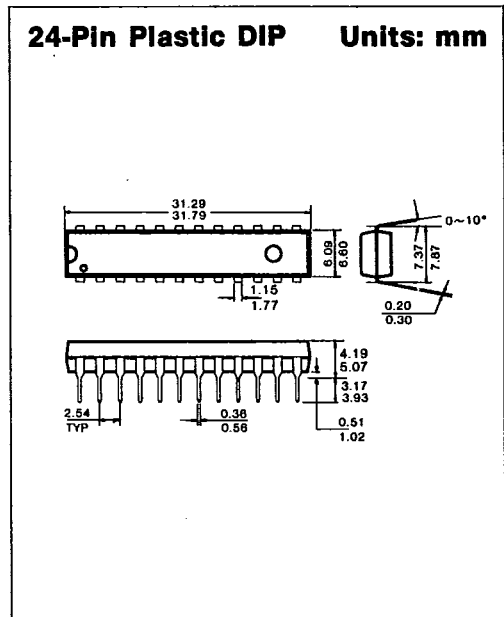
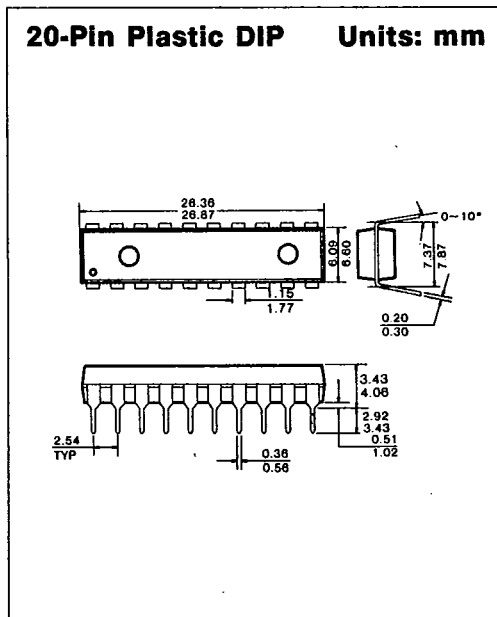
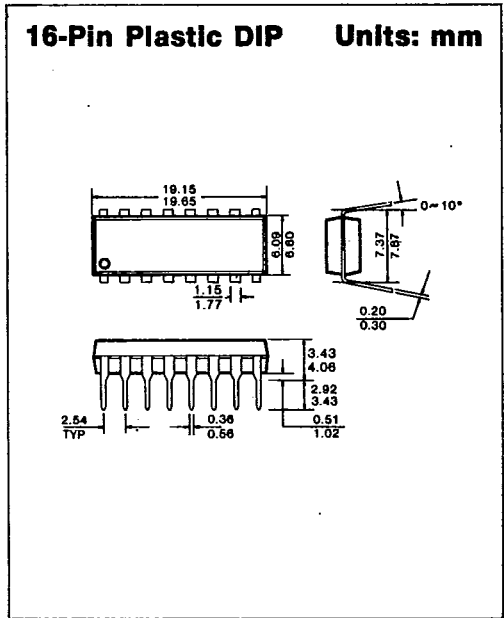
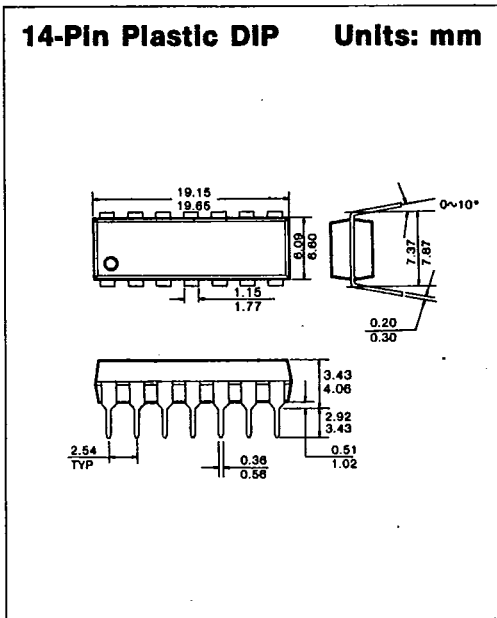
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PACKAGE DIMENSIONS

T-90-20

1. PLASTIC PACKAGES



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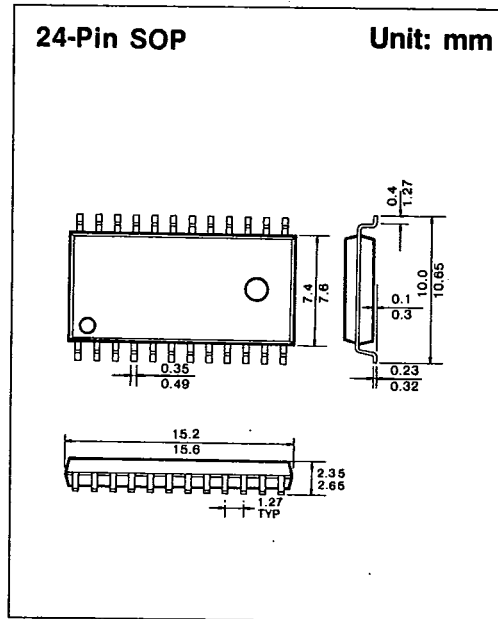
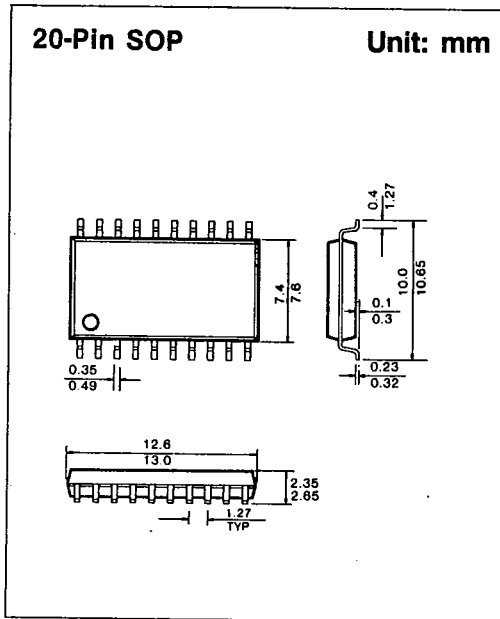
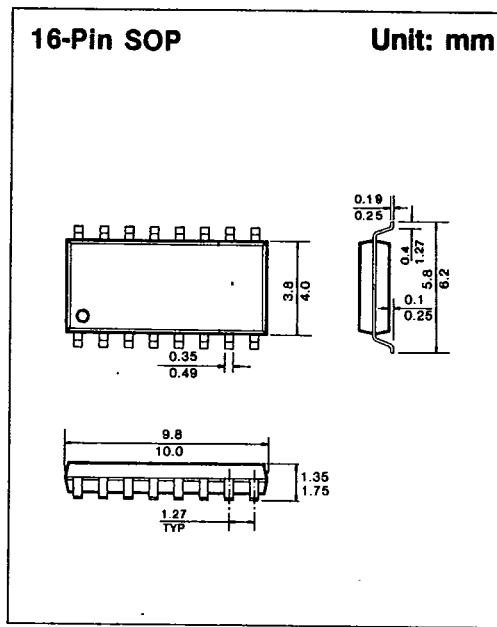
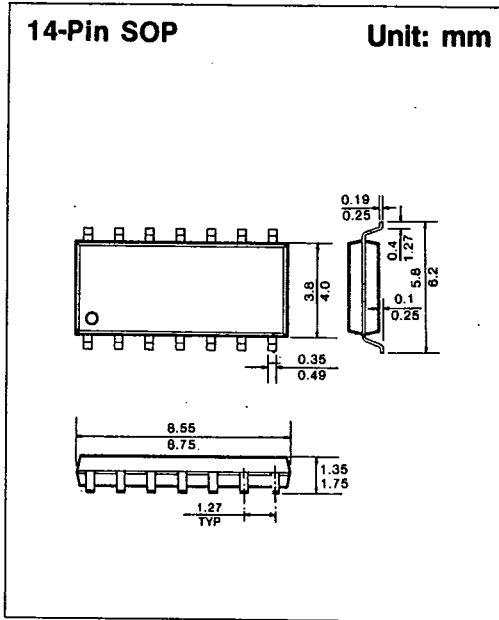
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PACKAGE DIMENSIONS

T-90-20



PACKAGE DIMENSIONS

T-90-20

2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	8.10	7.49
E ₁	7.82	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	8.10	7.49
E ₁	7.82	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	25.78	26.33
E	8.10	8.60
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	31.50	32.84
E	7.24	7.75
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.776
S	1.85	1.93

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