

SN54HCT04, SN74HCT04 HEX INVERTERS

SCLS042B – JULY 1986 – REVISED MAY 1997

- Inputs Are TTL-Voltage Compatible
- Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

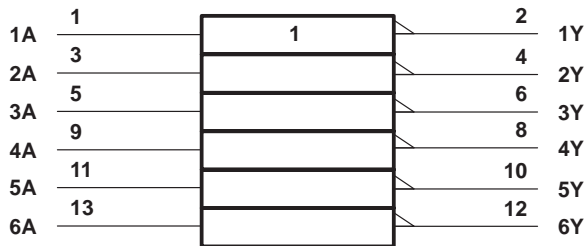
These devices contain six independent inverters. They perform the Boolean function $Y = \bar{A}$ in positive logic.

The SN54HCT04 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HCT04 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



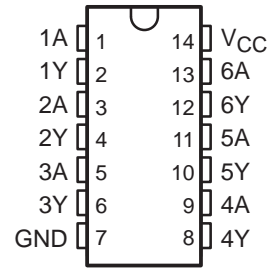
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, N, and PW packages.

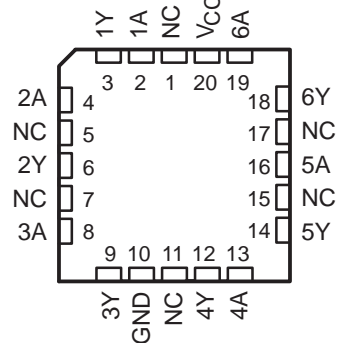
logic diagram (positive logic)



SN54HCT04 . . . J OR W PACKAGE
SN74HCT04 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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INSTRUMENTS**

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SN54HCT04, SN74HCT04 HEX INVERTERS

SCLS042B – JULY 1986 – REVISED MAY 1997

absolute maximum ratings over operating free-air temperature†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	127°C/W
N package	78°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		SN54HCT04			SN74HCT04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V			2			V
V_{IL}	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V			0	0.8	0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	0		500	0		500	ns
T_A	Operating free-air temperature	-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT04		SN74HCT04		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	4.5 V	$I_{OH} = -20 \mu\text{A}$	4.4	4.499	4.4	4.4	V		
			$I_{OH} = -4 \text{ mA}$	3.98	4.3	3.7	3.84			
V_{OL}	$V_I = V_{IH}$ or V_{IL}	4.5 V	$I_{OL} = 20 \mu\text{A}$	0.001	0.1	0.1	0.1	V		
			$I_{OL} = 4 \text{ mA}$	0.17	0.26	0.4	0.33			
I_I	$V_I = V_{CC}$ or 0	5.5 V	± 0.1	± 100	± 1000	± 1000	nA			
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	5.5 V		2	40	20	μA			
ΔI_{CC}^\ddagger	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}	5.5 V	1.4	2.4	3	2.9	mA			
C_i		4.5 V to 5.5 V	3	10	10	10	pF			

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .



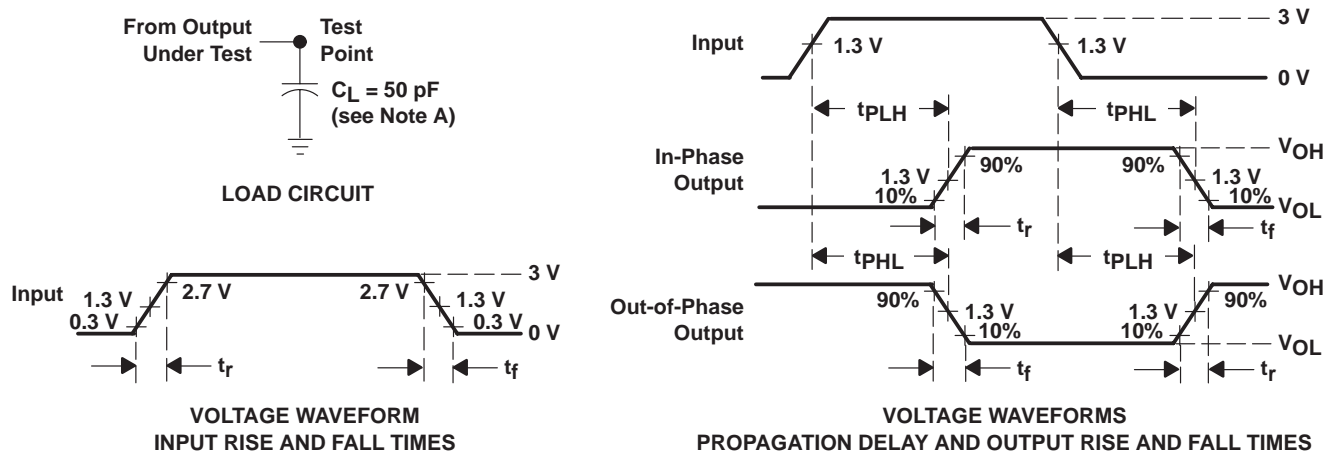
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT04		SN74HCT04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		14	20		30		25	ns
			5.5 V		13	18		27		23	
t_t		Y	4.5 V		9	15		22		19	ns
			5.5 V		8	14		20		17	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per inverter	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - C. The outputs are measured one at a time with one input transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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SN74HCT04, Hex Inverters

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54HCT04	SN74HCT04
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	CMOS	CMOS
Output Drive (mA)		-4/4
No. of Gates	6	6
Static Current		0.02
tpd max (ns)		23

FEATURES

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DESCRIPTION

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These devices contain six independent inverters. They perform the Boolean function $Y = A\$ in positive logic.

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TECHNICAL DOCUMENTS

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DATASHEET

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Full datasheet in Acrobat PDF: [sn74hct04.pdf](#) (65 KB, Rev.B) (Updated: 05/01/1997)

APPLICATION NOTES

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View Application Notes for [Digital Logic](#)

- [CMOS Power Consumption and CPD Calculation \(Rev. B\)](#) (SCAA035B - Updated: 06/01/1997)
- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Implications of Slow or Floating CMOS Inputs \(Rev. C\)](#) (SCBA004C - Updated: 02/01/1998)
- [SN54/74HCT CMOS Logic Family Applications and Restrictions](#) (SCLA011 - Updated: 05/01/1996)
- [Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc](#) (SCLA008 - Updated: 04/01/1996)

RELATED DOCUMENTS

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- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74HCT04D	SOP (D)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74HCT04N	PDIP (N)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74HCT04PWR	TSSOP (PW)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY SUS	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74HCT04APWLE	OBSOLETE	TSSOP (PW) 14	-40 TO 85	View Contents	1KU		N/A*		Not Available			
SN74HCT04D	ACTIVE	SOP (D) 14	-40 TO 85	View Contents	1KU 0.18	50	N/A*	>10k 18 Oct	4 WKS	Avnet AMERICA	> 1k	BUY NOW
								>10k 22 Oct		DigiKey AMERICA	> 1k	BUY NOW
SN74HCT04DR	ACTIVE	SOP (D) 14	-40 TO 85	View Contents	1KU 0.18	2500	N/A*	>10k 15 Oct	4 WKS	Avnet AMERICA	> 1k	BUY NOW
								>10k 16 Oct		DigiKey AMERICA	> 1k	BUY NOW
								10k 21 Oct				
								>10k 28 Oct				
SN74HCT04N	ACTIVE	PDIP (N) 14	-40 TO 85	View Contents	1KU 0.18	25	N/A*		6 WKS	Avnet AMERICA	> 1k	BUY NOW
										DigiKey AMERICA	580	BUY NOW
SN74HCT04NSR	ACTIVE	SOP (NS) 14		View Contents	1KU 0.24	2000	N/A*	1474 03 Oct	6 WKS			

SN74HCT04PWLE	OBSOLETE	TSSOP (PW) 14	-40 TO 85	View Contents	1KU		N/A*		Not Available			
SN74HCT04PWR	ACTIVE	TSSOP (PW) 14	-40 TO 85	View Contents	1KU 0.18	2000	N/A*	10k 17 Oct	4 WKS			
								>10k 28 Oct				

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