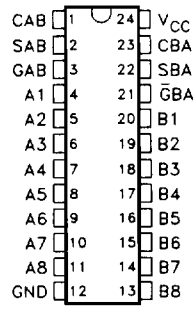
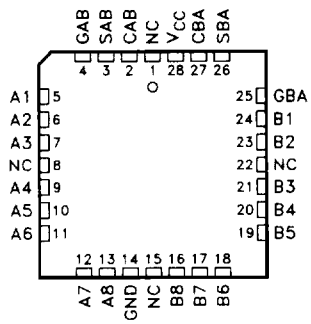
AUGUST 1989

- **State of the Art BICMOS Design Significantly Reduces I_{CCZ}**
- **Dependable Texas Instruments Quality and Reliability**
- **Bus Transceivers/Registers**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT652 ... JT PACKAGE
SN74BCT652 ... DW OR NT PACKAGE
(TOP VIEW)



SN54BCT652 ... FK PACKAGE
(TOP VIEW)



description

These devices consist of bus transceivers circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{G}BA$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}BA$. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The SN54BCT652 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT652 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, Hold B
H	H	↑	↑	X/	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, Store B
L	L	↑	↑	X	X/	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

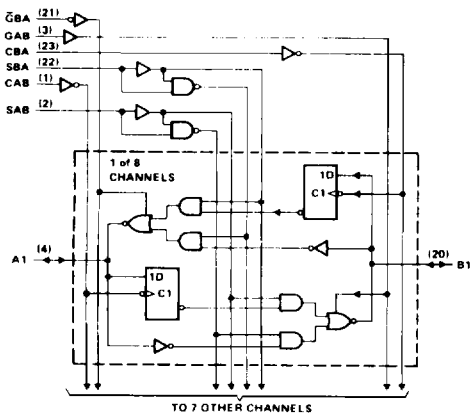
‡ The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input function are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock i.

/ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

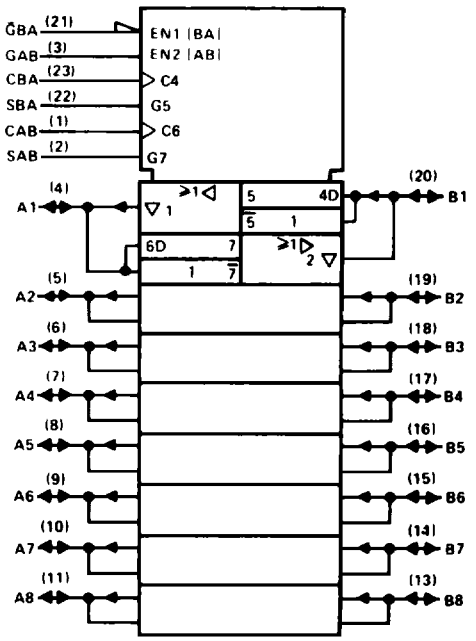
2

BiCMOS Circuits

logic diagram (positive logic)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for JT, DW, or NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage (I/O ports) ..... −0.5 V to 5.5 V
Input voltage (Excluding I/O ports) ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT652 ..... 96 mA
SN74BCT652 ..... 128 mA
Operating free-air temperature range: SN54BCT652 ..... −55°C to 125°C
SN74BCT652 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54BCT652			SN74BCT652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT652			SN74BCT652			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
			I_{OL} = 64 mA					0.42	0.55	
I_I	Control Inputs	V_{CC} = 5.5 V, V_I = 5.5 V				1			1	mA
	A or B	V_{CC} = 5.5 V, V_I = 5.5 V				1			1	
I_{IH}‡	Control Inputs	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
	A or B	V_{CC} = 5.5 V, V_I = 2.7 V				70			70	
I_{IL}‡	Control Inputs	V_{CC} = 5.5 V, V_I = 0.5 V				−1			−1	mA
	A or B	V_{CC} = 5.5 V, V_I = 0.5 V				−1			−1	
I_{OS}§		V_{CC} = 5.5 V, V_O = 0 V		−100		−225	−100		−225	mA
I_{CCL}		V_{CC} = 5.5 V, V_I = GND			43	69		43	69	mA
I_{CCH}		V_{CC} = 5.5 V, V_I = 4.5 V			6	10		6	10	mA
I_{CCZ}		V_{CC} = 5.5 V, V_I = GND			10	17		10	17	mA
C_i		V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			6			6		pF
C_{io}		V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			14			14		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'BCT652		SN54BCT652		SN74BCT652		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	77	0	77	0	77	MHz
t_w	Pulse duration	CBA or CAB high	6.5		6.5		6.5		ns
		CBA or CAB low	6.5		6.5		6.5		
t_{su}	Setup time, before CAB ↑ or CBA ↑	A or B	5		5		5		ns
t_h	Hold time, after CAB ↑ or CBA ↑	A or B	1		1		1		ns

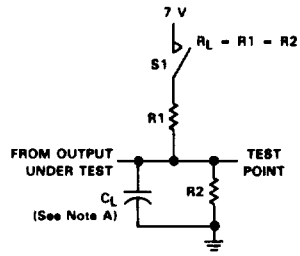
† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operation Conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT652			SN54BCT652		SN74BCT652		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			77			77		77		MHz
t_{PLH}	CBA	A	2.6	6.9	8.9	2.6	11.6	2.6	10.5	ns
t_{PHL}			2.8	6.8	8.8	2.8	10.7	2.8	9.9	
t_{PLH}	CAB	B	2.6	6.9	8.9	2.6	11.6	2.6	10.5	ns
t_{PHL}			2.8	6.8	8.8	2.8	10.7	2.8	9.9	
t_{PLH}	A	B	1.7	5.8	7.5	1.7	10.3	1.7	8.9	ns
t_{PHL}			2.4	6.5	8.2	2.4	10	2.4	9.8	
t_{PLH}	B	A	1.7	5.8	7.5	1.7	10.3	1.7	8.9	ns
t_{PHL}			2.4	6.5	8.2	2.4	10	2.4	9.8	
t_{PLH}	SBA‡ (with B high)	A	3.5	8.8	10.8	3.5	14.2	3.5	13.1	ns
t_{PHL}			2.4	5.9	7.7	2.4	9.1	2.4	8.5	
t_{PLH}	SBA‡ (with B low)	A	3	7.6	9.7	3	12.4	3	11.3	ns
t_{PHL}			3.8	8.3	10.4	3.8	12.9	3.8	12.5	
t_{PLH}	SAB‡ (with A high)	B	3.5	8.8	10.8	3.5	14.2	3.5	13.1	ns
t_{PHL}			2.4	5.9	7.7	2.4	9.1	2.4	8.5	
t_{PLH}	SAB‡ (with A low)	B	3	7.6	9.7	3	12.4	3	11.3	ns
t_{PHL}			3.8	8.3	10.4	3.8	12.9	3.8	12.5	
t_{PZH}	$\overline{G}$BA	A	2.5	7.2	8.9	2.5	11.2	2.5	10.6	ns
t_{PZL}			3.2	8.1	10.1	3.2	12.6	3.2	12	
t_{PHZ}	$\overline{G}$BA	A	2.8	6.7	8.8	2.8	10.9	2.8	10	ns
t_{PLZ}			2.4	6.3	8.4	2.4	10.5	2.4	9.5	
t_{PZH}	GAB	B	1.5	5.4	7.1	1.5	8.7	1.5	8.1	ns
t_{PZL}			2.3	6.2	8.1	2.3	9.9	2.3	9.3	
t_{PHZ}	GAB	B	3.5	8.2	10	3.5	12.2	3.5	11.6	ns
t_{PLZ}			2.8	7.2	9.5	2.8	12	2.8	11.3	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

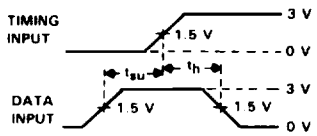
PARAMETER MEASUREMENT INFORMATION



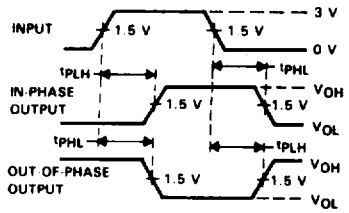
LOAD CIRCUIT

SWITCH POSITION TABLE

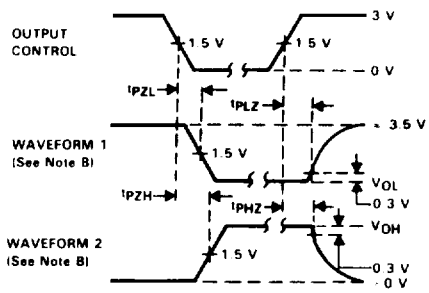
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 2.5 ns, t_f = 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265