GD54/74LS75

4-BIT BISTABLE LATCH

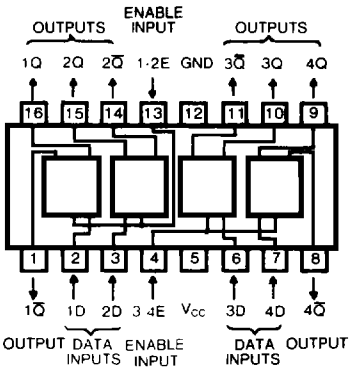
Features

- Enable inputs common to two circuits each
- Q ad $\overline{Q}$ outputs

Description

This device contains 4 D-type latch circuits and is provided with enable inputs E common to 2 circuits each. When E is high, the information from the data input D appears in the outputs Q and $\overline{Q}$. When the D signal changes, the signal that appears in outputs Q and $\overline{Q}$ also changes. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of Q and $\overline{Q}$ does not change even if D is changed.

Pin Configuration



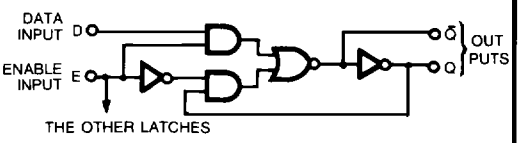
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (Note 1)

E	D	Q	$\overline{Q}$
H	H	H	L
H	L	L	H
L	X	Q^0	$\overline{Q}^0$

Note 1 Q^0 $\overline{Q}^0$ Level of Q and $\overline{Q}$ before the indicated steady-state input conditions were established
X Irrelevant

Block Diagram (Each Latch)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
t_W	Width of enable pulse		20			ns
t_{SU}	Set up time		20			ns
t_h	Hold time		5			ns
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max, V_{IH}=Min	54	2.5	3.5		V
				74	2.7	3.5		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	D				0.1	mA
			E				0.4	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	D				20	μA
			E				80	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	D				−0.4	mA
			E				−1.6	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				6.3	12	mA

Note 1 All typicals are at V_{CC}=5V, T_A=25°C
Note 2 Not more than one output should be shorted at a time, and the duration should not exceed one second
Note 3. I_{CC} is measured with all outputs open and all inputs grounded

Switching Characteristics, V_{CC}=5V, T_A=25°, unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D to output Q	C_L=15pF, R_L=2kΩ		15	27	ns
t_{PHL}				9	17	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D to output $\overline{Q}$			12	20	ns
t_{PHL}				7	15	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation Time, from input E to output Q			15	27	ns
t_{PHL}				14	25	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E to output $\overline{Q}$			16	30	ns
t_{PHL}				7	15	ns