	Tentative	DRAF115E	
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DRAF115E

Silicon PNP epitaxial planar type

For digital circuits

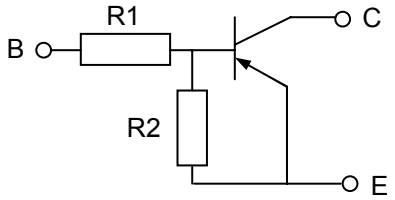
Marking Symbol : LN

Package Code : ML3-N4-B

Absolute Maximum Ratings Ta = 25 °C

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	VCBO	-50	V
Collector-emitter voltage (Base open)	VCEO	-50	V
Collector current	IC	-100	mA
Total power dissipation	PT	100	mW
Junction temperature	Tj	150	°C
Storage temperature	Tstg	-55 to +150	°C

Internal Connection



Resistance value	R1	100	kΩ
	R2	100	kΩ
Pin name	1.	Base	
	2.	Emitter	
	3.	Collector	

Electrical Characteristics Ta = 25 °C±3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	VCBO	IC = -10 µA, IE = 0	-50			V
Collector-emitter voltage (Base open)	VCEO	IC = -2 mA, IB = 0	-50			V
Collector-base cutoff current (Emitter open)	ICBO	VCB = -50 V, IE = 0			-0.1	µA
Collector-emitter cutoff current (Base open)	ICEO	VCE = -50 V, IB = 0			-0.5	µA
Emitter-base cutoff current (Collector open)	IEBO	VEB = -6 V, IC = 0			-0.1	mA
Forward current transfer ratio	hFE	VCE = -10 V, IC = -5 mA	80			-
Collector-emitter saturation voltage	VCE(sat)	IC = -10 mA, IB = -0.5 mA			-0.25	V
Input voltage	Vi(on)	VCE = -0.2 V, IC = -5 mA	-5.7			V
	Vi(off)	VCE = -5 V, IC = -100 µA			-0.8	
Input resistance	R1		-30%	100	+30%	kΩ
Resistance ratio	R1/R2		0.8	1.0	1.2	-

Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

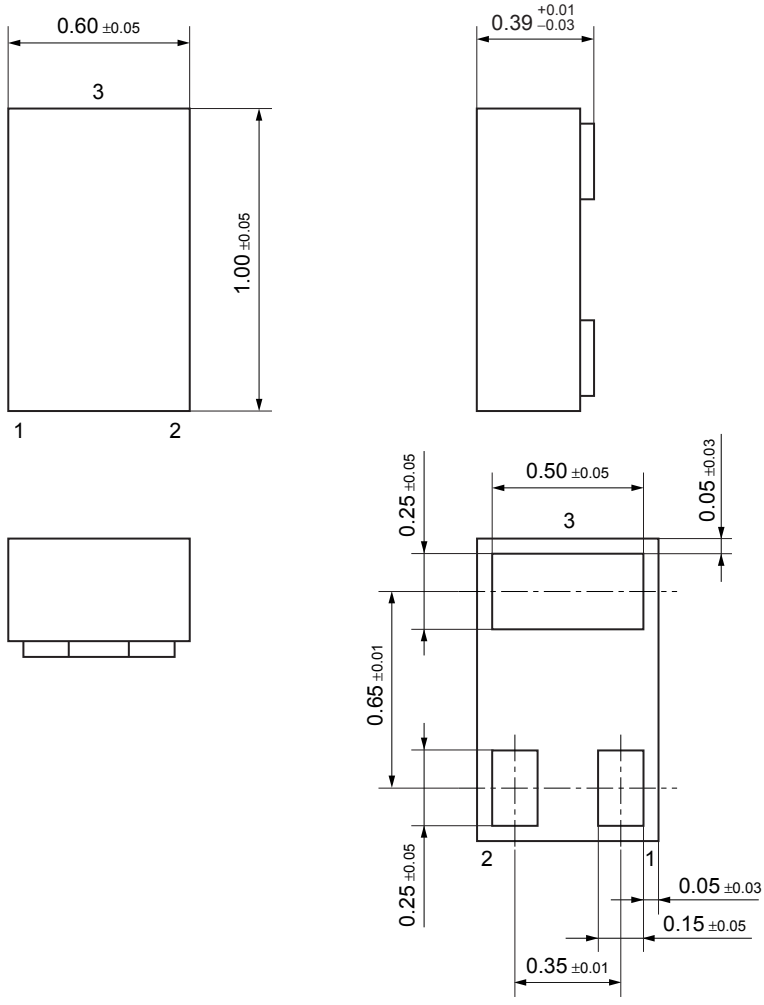
Packing

Embossed type (Thermo-compression sealing) : 10 000 pcs / reel

2010.2.25	2010.7.9	
Prepared	Revised	

ML3-N4-B

Unit: mm



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