# 54H/74H78 01520
# 54LS/74LS78 01519

## DUAL JK FLIP-FLOP

(With Common Clear and Clock and Separate Set Inputs)

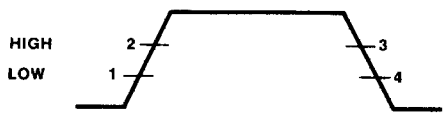
**DESCRIPTION** — The 'H78 is a dual JK master/slave flip-flop with separate Direct Set inputs, a common Direct Clear input and a common Clock Pulse input. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) isolate slave from mas-2ter; 2) enter information from J and K inputs to master; 3) disable J and K inputs; 4) transfer information from master to slave. The logic state of the J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

**TRUTH TABLE**

| INPUTS | | OUTPUT |
|---|---|---|
| @ $t_n$ | | @ $t_{n+1}$ |
| J | K | Q |
| L | L | $Q_n$ |
| L | H | L |
| H | L | H |
| H | H | $\overline{Q}_n$ |

H = HIGH Voltage Level
L = LOW Voltage Level
$t_n$ = Bit time before clock pulse.
$t_{n+1}$ = Bit time after clock pulse.

**CLOCK WAVEFORM**



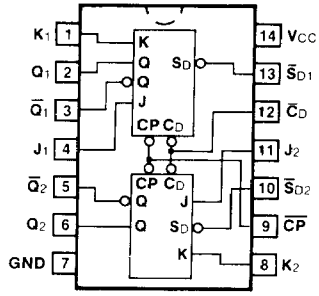

Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ is makes both Q and $\overline{Q}$ HIGH

The 'LS78 is a dual JK, negative edge-triggered flip-flop which also offers separate Direct Set inputs, a common Direct Clear and common Clock Pulse input. When the Clock Pulse input is HIGH, the JK inputs are enabled and data is accepted. This data will be transferred to the outputs according to the Truth Table on the HIGH-to-LOW clock transitions.

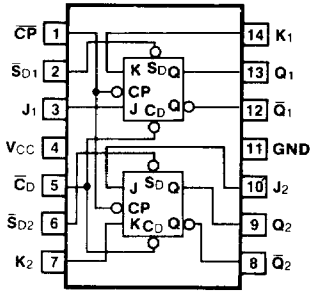
**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE: $V_{CC}$ = +5.0 V ±5%, $T_A$ = 0°C to +70°C | MILITARY GRADE: $V_{CC}$ = +5.0 V ±10%, $T_A$ = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 74H78PC | | 9A |
| | B | 74LS78PC | | |
| Ceramic DIP (D) | A | 74H78DC | 54H78DM | 6A |
| | B | 74LS78DC | 54LS78DM | |
| Flatpak (F) | A | 74H78FC | 54H78FM | 3I |
| | B | 74LS78FC | 54LS78FM | |

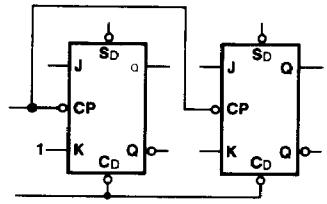
**CONNECTION DIAGRAMS**
PINOUT A




PINOUT B




**LOGIC SYMBOL**

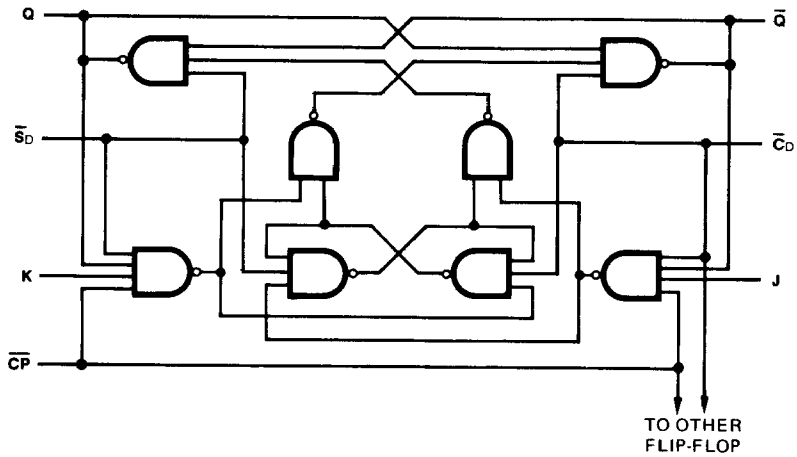



VCC = Pin 14 (4)
GND = Pin 7 (11)

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES | DESCRIPTION | 54/74H (U.L.) HIGH/LOW | 54/74LS (U.L.) HIGH/LOW |
|---|---|---|---|
| $J_1$, $J_2$, $K_1$, $K_2$ | Data Inputs | 1.25/1.25 | 0.5/0.25 |
| $\overline{CP}$ | Clock Pulse Input (Active Falling Edge) | 2.5/2.5 | 4.0/1.0 |
| $\overline{C}_D$ | Direct Clear Input (Active LOW) | 5.0/5.0 | 3.0/1.0 |
| $\overline{S}_{D1}$, $\overline{S}_{D2}$ | Direct Set Inputs (Active LOW) | 2.5/2.5 | 1.5/0.5 |
| $Q_1$, $\overline{Q}_1$, $Q_2$, $\overline{Q}_2$ | Outputs | 12.5/12.5 | 10/5.0 (2.5) |

**LOGIC DIAGRAM**
(one half shown)




**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL | PARAMETER | 54/74H Min | 54/74H Max | 54/74LS Min | 54/74LS Max | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Power Supply Current | | 50 | | 8.0 | mA | $V_{CC}$ = Max, $V_{CP}$ = 0 V |

**AC CHARACTERISITICS:** $V_{CC}$ = +5.0 V, $T_A$ = +25°C (See Section 3 for waveforms and load configurations)

| SYMBOL | PARAMETER | 54/74H $C_L$ = 25 pF, $R_L$ = 280 Ω Min | 54/74H Max | 54/74LS $C_L$ = 15 pF Min | 54/74LS Max | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Clock Frequency | 25 | | 30 | | MHz | Figs. 3-1, 3-9 |
| $t_{PLH}$ | Propagation Delay | | 21 | | 20 | ns | Figs. 3-1, 3-9 |
| $t_{PHL}$ | $\overline{CP}$ to $Q_n$ or $\overline{Q}_n$ | | 27 | | 30 | | |
| $t_{PLH}$ | Propagation Delay | | 13 | | 20 | ns | Figs. 3-1, 3-10 |
| $t_{PHL}$ | $\overline{C}_D$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$ | | 24 | | 30 | | |

**AC OPERATING REQUIREMENTS:** $V_{CC}$ = +5.0 V, $T_A$ = +25°C

| SYMBOL | PARAMETER | 54/74H | | 54/74LS | | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $t_s$ (H) | Setup Time HIGH $J_n$ or $K_n$ to $\overline{CP}$ | 0 | | 20 | | ns | Fig. 3-18 ('H78)<br>Fig. 3-7 ('LS78) |
| $t_h$ (H) | Hold Time HIGH $J_n$ or $K_n$ to $\overline{CP}$ | 0 | | 0 | | ns | |
| $t_s$ (L) | Setup Time LOW $J_n$ or $K_n$ to $\overline{CP}$ | 0 | | 20 | | ns | |
| $t_h$ (L) | Hold Time LOW $J_n$ or $K_n$ to $\overline{CP}$ | 0 | | 0 | | ns | |
| $t_w$ (H)<br>$t_w$ (L) | $\overline{CP}$ Pulse Width | 12<br>28 | | 20<br>13.5 | | ns | Fig. 3-9 |
| $t_w$ (L) | $\overline{C}_D$ or $\overline{S}_{Dn}$ Pulse Width LOW | 16 | | 25 | | ns | Fig. 3-10 |