

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R184-97. – CFS	97-02-24	Monica L. Poelking
B	Changes in accordance with NOR 5962-R396-97. - RLC	97-07-29	Raymond L. Monnin
C	Add device class T criteria. Editorial changes throughout. JAK	98-12-07	Monica L. Poelking
D	Correct the total dose rate and update RHA levels. - LTG	99-04-28	Monica L. Poelking
E	Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. – LTG	05-09-07	Thomas M. Hess

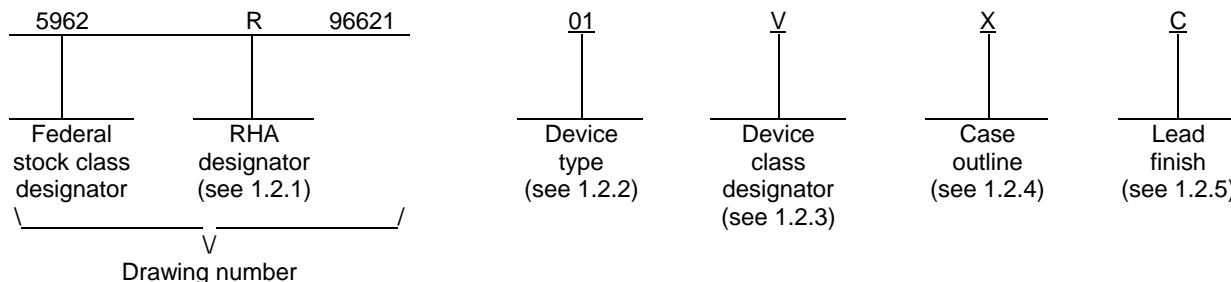
REV																				
SHEET																				
REV	E	E	E	E	E	E	E	E	E	E	E									
SHEET	15	16	17	18	19	20	21	22	23	24	25									
REV STATUS				REV	E	C	D	E	E	E	E	D	C	C	E	E	E	E		
OF SHEETS				SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A	PREPARED BY Dan Wonnell	<b>DEFENSE SUPPLY CENTER COLUMBUS</b> <b>COLUMBUS, OHIO 43218-3990</b> <a href="http://www.dscc.dla.mil">http://www.dscc.dla.mil</a>  <b>MICROCIRCUIT, DIGITAL, RADIATION HARDENED, CMOS, NAND GATES, MONOLITHIC SILICON</b>																	
<b>STANDARD MICROCIRCUIT DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Monica L. Poelking																		
	APPROVED BY Monica L. Poelking																		
	DRAWING APPROVAL DATE 95-11-27																		
AMSC N/A	REVISION LEVEL E	SIZE <b>A</b>	CAGE CODE <b>67268</b>	<b>5962-96621</b>															
		SHEET 1 OF 25																	

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device classes Q and M), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	4011B	Radiation hardened, CMOS, quad 2-input NAND gate
02	4012B	Radiation hardened, CMOS, dual 4-input NAND gate
03	4023B	Radiation hardened, CMOS, triple 3-input NAND gate
04	4011BN	Radiation hardened, CMOS, quad 2-input NAND gate with neutron irradiated die
05	4012BN	Radiation hardened, CMOS, dual 4-input NAND gate with neutron irradiated die
06	4023BN	Radiation hardened, CMOS, triple 3-input NAND gate with neutron irradiated die

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
C	CDIP2-T14	14	Dual-in-line
X	CDFP3-F14	14	Flat pack

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1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range ( $V_{DD}$ ) .....	-0.5 V dc to +20 V dc
DC input voltage range ( $V_{IN}$ ) .....	-0.5 V dc to $V_{DD} + 0.5$ V dc
DC input current, any one input ( $I_{IN}$ ) .....	$\pm 10$ mA
Device dissipation per output transistor .....	100 mW
Storage temperature range ( $T_{STG}$ ) .....	-65°C to +150°C
Lead temperature (soldering, 10 seconds).....	+265°C
Thermal resistance, junction-to-case ( $\Theta_{JC}$ ):	
Case outline C .....	24°C/W
Case outline X.....	30°C/W
Thermal resistance, junction-to-ambient ( $\Theta_{JA}$ ):	
Case outline C .....	74°C/W
Case outline X.....	116°C/W
Junction temperature ( $T_J$ ) .....	+175°C
Maximum package power dissipation at $T_A = +125^\circ\text{C}$ ( $P_D$ ): 4/	
Case outline C .....	0.68 W
Case outline X.....	0.43 W

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range ( $V_{DD}$ ) .....	+3.0 V dc to +18 V dc
Case operating temperature range ( $T_C$ ) .....	-55°C to +125°C
Input voltage range ( $V_{IN}$ ) .....	+0.0 V to $V_{DD}$
Output voltage range ( $V_{OUT}$ ).....	+0.0 V to $V_{DD}$

1.5 Radiation features:

Maximum total dose available (dose rate = 50 – 300 rad (Si)/s) .....	$1 \times 10^5$ Rads (Si)
Single event phenomenon (SEP) effective	
linear energy threshold (LET), no upsets (see 4.4.4.5) .....	$> 75$ MeV/(cm <sup>2</sup> /mg) 5/
Dose rate upset (20 ns pulse) .....	$> 5 \times 10^8$ Rads (Si)/s 5/
Dose rate latch-up.....	$> 2 \times 10^8$ Rads(Si)/s 5/
Dose rate survivability .....	$> 5 \times 10^{11}$ Rads (Si)/s 5/
Neutron irradiated (device types 04, 05, and 06) .....	$1 \times 10^{14}$ neutrons/cm <sup>2</sup> 5/

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Unless otherwise noted, all voltages are referenced to  $V_{SS}$ .
- 3/ The limits for the parameters specified herein shall apply over the full specified  $V_{DD}$  range and case temperature range of -55°C to +125°C unless otherwise noted.
- 4/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on  $\Theta_{JA}$ ) at the following rate:  
    Case outline C .....
 13.5 mW/°C || Case outline X ..... | 8.6 mW/°C |

5/ Guaranteed by design or process but not tested.

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## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

### DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Irradiation test connections. The irradiation test connections shall be as specified in table III.

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3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q, T, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 36 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Supply current	I <sub>DD</sub>	V <sub>DD</sub> = 20 V, V <sub>IN</sub> = V <sub>DD</sub> or GND	All	1		0.5	μA
					M, D, P, L, R 2/		
		V <sub>DD</sub> = 18 V, V <sub>IN</sub> = V <sub>DD</sub> or GND		1			
				3		0.5	
		V <sub>DD</sub> = 5 V, V <sub>IN</sub> = V <sub>DD</sub> or GND 1/		1, 3		0.25	
				2		7.5	
		V <sub>DD</sub> = 10 V, V <sub>IN</sub> = V <sub>DD</sub> or GND 1/		1, 3		0.5	
				2		15.0	
		V <sub>DD</sub> = 15 V, V <sub>IN</sub> = V <sub>DD</sub> or GND 1/		1, 3		0.5	
2			30.0				
Input leakage current low	I <sub>IL</sub>	V <sub>DD</sub> = 20 V, V <sub>IN</sub> = V <sub>DD</sub> or GND	All	1	-100		nA
				2	-1000		
		V <sub>DD</sub> = 18 V, V <sub>IN</sub> = V <sub>DD</sub> or GND		3	-100		
Input leakage current high	I <sub>IH</sub>	V <sub>DD</sub> = 20 V, V <sub>IN</sub> = V <sub>DD</sub> or GND	All	1		100	
				2		1000	
		V <sub>DD</sub> = 18 V, V <sub>IN</sub> = V <sub>DD</sub> or GND		3		100	
Output voltage low	V <sub>OL</sub>	V <sub>DD</sub> = 15 V, no load	All	1, 2, 3		50.0	mV
		V <sub>DD</sub> = 5 V, no load 1/				50.0	
		V <sub>DD</sub> = 10 V, no load 1/				50.0	
Output voltage high	V <sub>OH</sub>	V <sub>DD</sub> = 15 V, no load 3/	All	1, 2, 3	14.95		V
		V <sub>DD</sub> = 5 V, no load 1/			4.95		
		V <sub>DD</sub> = 10 V, no load 1/			9.95		
Low level output current (sink)	I <sub>OL</sub>	V <sub>DD</sub> = 5 V V <sub>O</sub> = 0.4 V	All	1	0.53		mA
				2 1/	0.36		
				3 1/	0.64		
		V <sub>DD</sub> = 10 V V <sub>O</sub> = 0.5 V	1	1.4			
			2 1/	0.9			
			3 1/	1.6			
		V <sub>DD</sub> = 15 V V <sub>O</sub> = 1.5 V	1	3.5			
			2 1/	2.4			
			3 1/	4.2			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
High level output current (source)	I <sub>OH</sub>	V <sub>DD</sub> = 5 V V <sub>O</sub> = 4.6 V	All	1		-0.53	mA
				2 <u>1/</u>		-0.36	
				3 <u>1/</u>		-0.64	
		V <sub>DD</sub> = 5 V V <sub>O</sub> = 2.5 V	All	1		-1.8	
				2 <u>1/</u>		-1.15	
				3 <u>1/</u>		-2.0	
		V <sub>DD</sub> = 10 V V <sub>O</sub> = 9.5 V	All	1		-1.4	
				2 <u>1/</u>		-0.9	
				3 <u>1/</u>		-1.6	
		V <sub>DD</sub> = 15 V V <sub>O</sub> = 13.5 V	All	1		-3.5	
				2 <u>1/</u>		-2.4	
				3 <u>1/</u>		-4.2	
Low level input voltage	V <sub>IL</sub>	V <sub>DD</sub> = 5 V V <sub>OH</sub> > 4.5 V, V <sub>OL</sub> < 0.5 V	All	1, 2, 3		1.5	V
		V <sub>DD</sub> = 10 V V <sub>OH</sub> > 9.0 V, V <sub>OL</sub> < 1.0 V <u>1/</u>		1, 2, 3		3.0	
		V <sub>DD</sub> = 15 V V <sub>OH</sub> > 13.5 V, V <sub>OL</sub> < 1.5 V		1, 2, 3		4.0	
High level input voltage	V <sub>IH</sub>	V <sub>DD</sub> = 5 V V <sub>OH</sub> > 4.5 V, V <sub>OL</sub> < 0.5 V	All	1, 2, 3	3.5		
		V <sub>DD</sub> = 10 V V <sub>OH</sub> > 9.0 V, V <sub>OL</sub> < 1.0 V <u>1/</u>		1, 2, 3	7.0		
		V <sub>DD</sub> = 15 V V <sub>OH</sub> > 13.5 V, V <sub>OL</sub> < 1.5 V		1, 2, 3	11.0		
N threshold voltage	V <sub>NTH</sub>	V <sub>DD</sub> = 10 V, I <sub>SS</sub> = -10 μA M, D, P, L, R <u>2/</u>	All	1	-0.7	-2.8	V
					-0.2	-2.8	
N threshold voltage delta	ΔV <sub>NTH</sub>	V <sub>DD</sub> = 10 V, I <sub>SS</sub> = -10 μA M, D, P, L, R <u>2/</u>	All	1		±1.0	
P threshold	V <sub>PTH</sub>	V <sub>SS</sub> = 0.0 V, I <sub>DD</sub> = 10 μA M, D, P, L, R <u>2/</u>	All	1	0.7	2.8	V
					0.2	2.8	
P threshold voltage delta	ΔV <sub>PTH</sub>	V <sub>SS</sub> = 0.0 V, I <sub>DD</sub> = 10 μA M, D, P, L, R <u>2/</u>	All	1		±1.0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Functional tests		V <sub>DD</sub> = 2.8 V, V <sub>IN</sub> = V <sub>DD</sub> or GND	All	7	V <sub>OH</sub> > V <sub>DD</sub> /2	V <sub>OL</sub> < V <sub>DD</sub> /2	V
		V <sub>DD</sub> = 20 V, V <sub>IN</sub> = V <sub>DD</sub> or GND		7			
		V <sub>DD</sub> = 18 V, V <sub>IN</sub> = V <sub>DD</sub> or GND M, D, P, L, R <u>2/</u>	8A				
		V <sub>DD</sub> = 3.0 V, V <sub>IN</sub> = V <sub>DD</sub> or GND M, D, P, L, R <u>2/</u>	8B				
Input capacitance	C <sub>IN</sub>	Any input, see 4.4.1c <u>1/</u>	All	4		7.5	pF
Propagation delay time, any input to output	t <sub>PHL</sub> , t <sub>PLH</sub>	V <sub>DD</sub> = 5 V, V <sub>IN</sub> = V <sub>DD</sub> or GND <u>4/</u>		9		250	ns
		M, D, P, L, R <u>2/</u>		10, 11		338	
				9		338	
		V <sub>DD</sub> = 10 V <u>1/</u> <u>4/</u>		9		120	
		V <sub>DD</sub> = 15 V <u>1/</u> <u>4/</u>		9		90	
Transition time	t <sub>THL</sub> , t <sub>TLH</sub>	V <sub>DD</sub> = 5 V, V <sub>IN</sub> = V <sub>DD</sub> or GND <u>4/</u>	All	9		200	
				10, 11		270	
		V <sub>DD</sub> = 10 V <u>1/</u> <u>4/</u>		9		100	
		V <sub>DD</sub> = 15 V <u>1/</u> <u>4/</u>		9		80	

1/ These tests are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which affect these characteristics.

2/ Devices supplied to this drawing meet all levels M, D, P, L, and R of irradiation. However, this device is only tested at the "R" level (see 1.5 herein). Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T<sub>A</sub> = +25°C.

3/ For accuracy, voltage is measured differentially to V<sub>DD</sub>. Limit is 0.050 V maximum.

4/ C<sub>L</sub> = 50 pF, R<sub>L</sub> = 200 kΩ, input t<sub>r</sub>, t<sub>f</sub> < 20 ns.

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Device types	01, 04	02, 05	03, 06
Case outlines	C and X		
Terminal number	Terminal symbol		
1	A	$\overline{J = ABCD}$	A
2	B	A	B
3	$\overline{J = AB}$	B	D
4	$\overline{K = CD}$	C	E
5	C	D	F
6	D	NC	$\overline{K = DEF}$
7	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>
8	F	NC	C
9	$\overline{E}$	E	$\overline{J = ABC}$
10	$\overline{L = EF}$	F	$\overline{L = GHI}$
11	$\overline{M = GH}$	G	I
12	G	$\overline{H}$	H
13	H	$\overline{K = EFGH}$	G
14	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>

NC = No connection

FIGURE 1. Terminal connections.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-96621</b>
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Device types 01 and 04

Inputs		Outputs
A, C, E, and G	B, D, F, and H	J, K, L, and M
H	H	L
X	L	H
L	X	H

H = High voltage level  
 L = Low voltage level  
 X = Don't care

Device types 02 and 05

Inputs				Outputs
A, E	B, F	C, G	D, H	J, K
H	H	H	H	L
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H

H = High voltage level  
 L = Low voltage level  
 X = Don't care

Device types 03 and 06

Inputs			Outputs
A, D, G	B, E, H	C, F, I	J, K, L
H	H	H	L
X	X	L	H
X	L	X	H
L	X	X	H

H = High voltage level  
 L = Low voltage level  
 X = Don't care

FIGURE 2. Truth tables.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q, T, and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. For device classes Q, T, and V, interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B or as modified in the device manufacturer's Quality Management (QM) plan.

4.3 Qualification inspection for device classes Q, T, and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

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4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- c.  $C_{IN}$  shall be measured only for initial qualification and after process or design changes which may affect capacitance.  $C_{IN}$  shall be measured between the designated terminal and GND at a frequency of 1 MHz. Tests shall be sufficient to validate the limits defined in table I herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9	As specified in QM plan
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 <u>1/</u>	1, 2, 3, 7, 8, 9, 10, 11 <u>1/</u>	1, 2, 3, 7, 8, 9, 10, 11 <u>2/ 3/</u>	
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11 <u>3/</u>	
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9	
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9	

1/ PDA applies to subgroups 1 and 7.

2/ PDA applies to subgroups 1, 7, 9, and Δ's.

3/ Delta limits, as specified in table IIB herein, shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters (see table I).

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameters <u>1/</u>	Symbol	Delta limits
Supply current	$I_{DD}$	$\pm 0.1 \mu A$
Output current (sink) $V_{DD} = 5.0 V$	$I_{OL}$	$\pm 20\%$
Output current (source) $V_{DD} = 5.0 V, V_{OUT} = 4.6 V$	$I_{OH}$	$\pm 20\%$

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE III. Irradiation test connections.

Device types	Open	Ground	$V_{DD} = 10\text{ V} \pm 0.5\text{ V}$
01, 04	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12, 13, 14
02, 05	1, 6, 8, 13	7	2, 3, 4, 5, 9, 10, 11, 12, 14
03, 06	6, 9, 10	7	1, 2, 3, 4, 5, 8, 11, 12, 13, 14

NOTE: Each pin except  $V_{DD}$  and GND will have a resistor of  $47\text{ k}\Omega \pm 5\%$  for irradiation testing.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b.  $T_A = +125^\circ\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q, T, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535 and the end-point electrical parameters shall be as specified in table IIA herein. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. The end-point electrical parameters for class T devices shall be as specified in Table I, Group A subgroups, or as modified in the QM plan.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein. For device class T, the total dose requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535 (see 1.5 herein).

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4.4.4.1.1 Accelerated aging testing. Accelerated aging testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron irradiation. Neutron irradiation for device types 04, 05, and 06 shall be conducted in wafer form using a neutron fluence of approximately  $1 \times 10^{14}$  neutrons/cm<sup>2</sup>.

4.4.4.3 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein (see 1.5 herein). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein (see 1.5 herein).

- a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.
- b. Transient dose rate upset testing for class Q, T, and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.5 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class T and V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e.  $0^\circ \leq \text{angle} \leq 60^\circ$ ). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be  $\geq 100$  errors or  $\geq 10^6$  ions/cm<sup>2</sup>.
- c. The flux shall be between  $10^2$  and  $10^5$  ions/cm<sup>2</sup>/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be  $\geq 20$  micron in silicon.
- e. The test temperature shall be +25°C and the maximum rated operating temperature  $\pm 10^\circ\text{C}$ .
- f. Bias conditions shall be defined by the manufacturer for the latchup measurements.
- g. Test four devices with zero failures.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990 or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T, and V. Sources of supply for device classes Q, T, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

- a. RHA upset levels.
- b. Test conditions (SEP).
- c. Number of upsets (SEP).
- d. Number of transients (SEP).
- e. Occurrence of latchup (SEP).

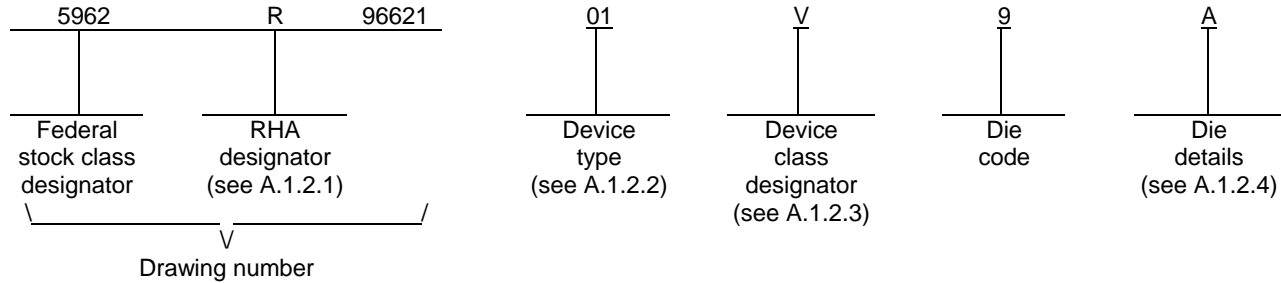
<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-96621</b>
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A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	4011B	Radiation hardened, CMOS, quad 2-input NAND gate
02	4012B	Radiation hardened, CMOS, dual 4-input NAND gate
03	4023B	Radiation hardened, CMOS, triple 3-input NAND gate
04	4011BN	Radiation hardened, CMOS, quad 2-input NAND gate with neutron irradiated die
05	4012BN	Radiation hardened, CMOS, dual 4-input NAND gate with neutron irradiated die
06	4023BN	Radiation hardened, CMOS, triple 3-input NAND gate with neutron irradiated die

A.1.2.3 Device class designator.

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

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A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

<u>Die type</u>	<u>Figure number</u>
01, 04	A-1
02, 05	A-2
03, 06	A-3

A.1.2.4.2 Die bonding pad locations and electrical functions.

<u>Die type</u>	<u>Figure number</u>
01, 04	A-1
02, 05	A-2
03, 06	A-3

A.1.2.4.3 Interface materials.

<u>Die type</u>	<u>Figure number</u>
01, 04	A-1
02, 05	A-2
03, 06	A-3

A.1.2.4.4 Assembly related information.

<u>Die type</u>	<u>Figure number</u>
01, 04	A-1
02, 05	A-2
03, 06	A-3

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

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DEPARTMENT OF DEFENSE HANDBOOKS

- MIL-HDBK-103 - List of Standard Microcircuit Drawings.
- MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figures A-1, A-2, and A-3.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figures A-1, A-2, and A-3.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figures A-1, A-2, and A-3.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figures A-1, A-2, and A-3.

A.3.2.5 Truth tables. The truth tables shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

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A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

- a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.
- b. 100% wafer probe (see paragraph A.3.4 herein).
- c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43218-3990 or telephone (614) 692-0547.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DSCC-VA and have agreed to this drawing.

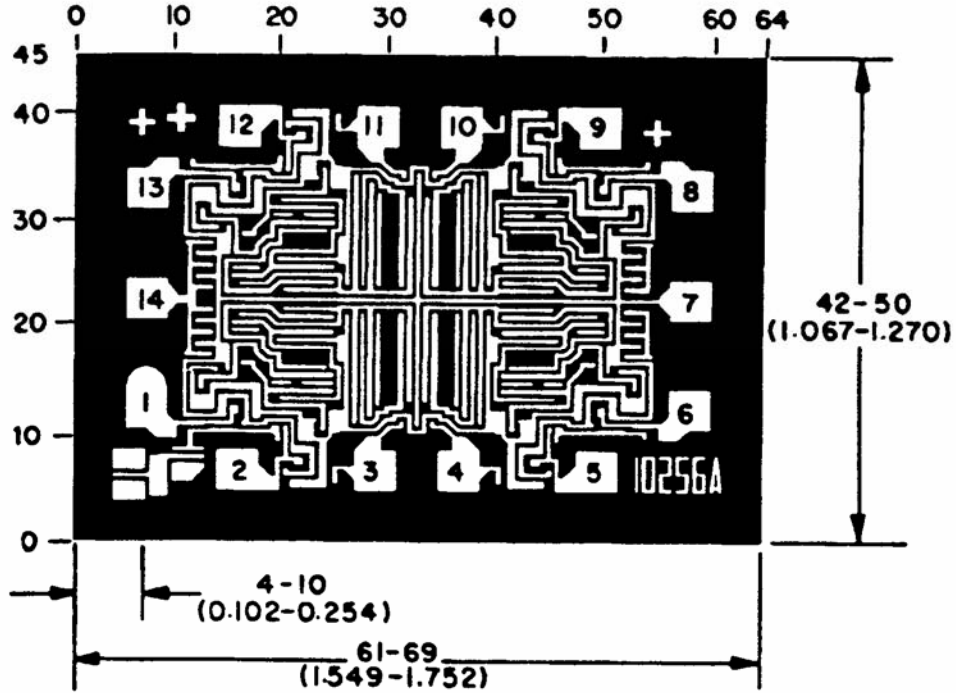
<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-96621</b>
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Die physical dimensions.

Die size: 1143 x 1626 microns.  
 Die thickness: 20 ±1 mils.

Die bonding pad locations and electrical functions.



NOTE: Pad numbers reflect terminal numbers when placed in case outlines C and X (see figure 1).

FIGURE A-1

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Interface materials.

Top metallization:       Al                   11.0 kÅ - 14.0 kÅ

Backside metallization:   None

Glassivation

Type:                PSG

Thickness:         10.4 kÅ – 15.6 kÅ

Substrate:                Single crystal silicon

Assembly related information.

Substrate potential:       Floating or tied to V<sub>DD</sub>

Special assembly  
instructions:                Bond pad #14 (V<sub>DD</sub>) first

FIGURE A-1 – Continued.

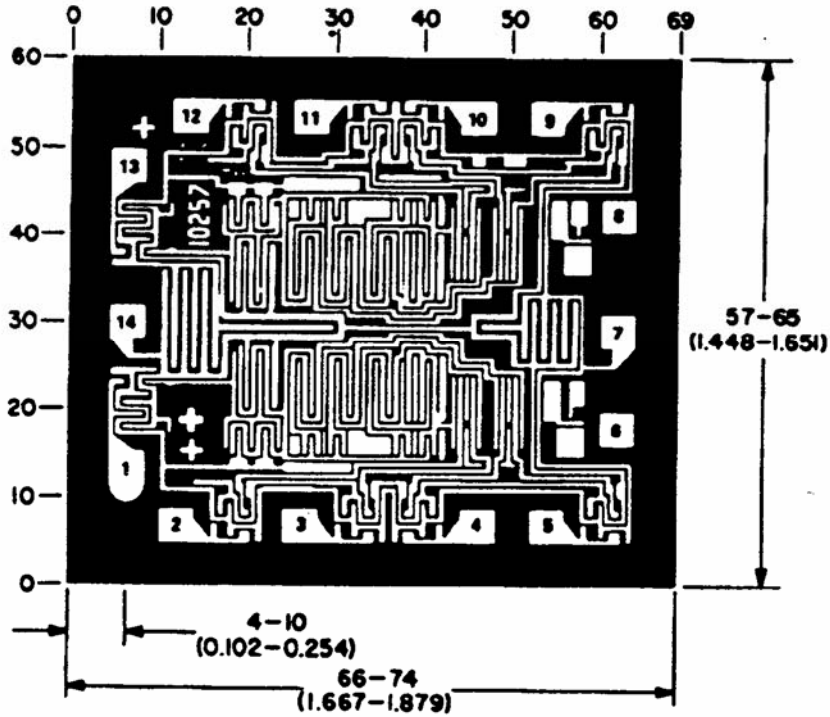
<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>	<b>5962-96621</b>
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Die physical dimensions.

Die size: 1524 x 1753 microns.  
 Die thickness: 20 ±1 mils.

Die bonding pad locations and electrical functions.



NOTE: Pad numbers reflect terminal numbers when placed in case outlines C and X (see figure 1).

FIGURE A-2

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Interface materials.

Top metallization:       Al                   11.0 kÅ - 14.0 kÅ

Backside metallization:   None

Glassivation

Type:                    PSG

Thickness:            10.4 kÅ – 15.6 kÅ

Substrate:                Single crystal silicon

Assembly related information.

Substrate potential:       Floating or tied to V<sub>DD</sub>

Special assembly  
instructions:                Bond pad #14 (V<sub>DD</sub>) first

FIGURE A-2 – Continued.

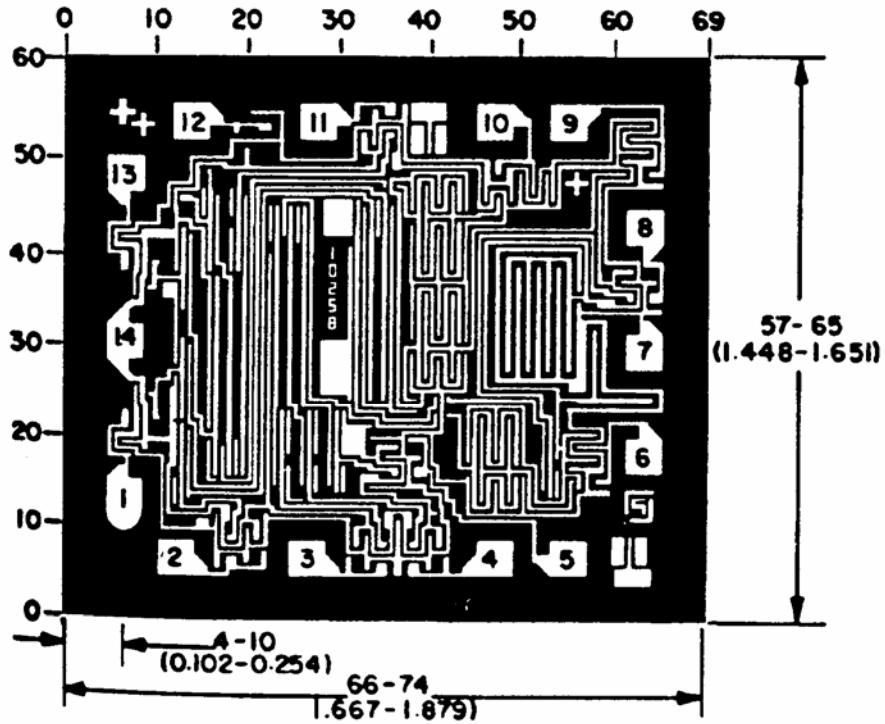
<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-96621</b>
		REVISION LEVEL <b>E</b>	SHEET 23

APPENDIX A  
 APPENDIX A FORMS A PART OF SMD 5962-96621

Die physical dimensions.

Die size: 1524 x 1753 microns.  
 Die thickness: 20 ±1 mils.

Die bonding pad locations and electrical functions.



NOTE: Pad numbers reflect terminal numbers when placed in case outlines C and X (see figure 1).

FIGURE A-3

<b>STANDARD          MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-96621</b>
		REVISION LEVEL E	SHEET 24



APPENDIX A  
APPENDIX A FORMS A PART OF SMD 5962-96621

Interface materials.

Top metallization:       Al                   11.0 kÅ - 14.0 kÅ

Backside metallization:   None

Glassivation

Type:                    PSG

Thickness:            10.4 kÅ – 15.6 kÅ

Substrate:                Single crystal silicon

Assembly related information.

Substrate potential:       Floating or tied to V<sub>DD</sub>

Special assembly  
instructions:                Bond pad #14 (V<sub>DD</sub>) first

FIGURE A-3 – Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>	<b>5962-96621</b>
	REVISION LEVEL <b>E</b>	SHEET 25

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-09-07

Approved sources of supply for SMD 5962-96621 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/SMCR/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962R9662101VCC	34371	CD4011BDMSR
5962R9662101VXC	34371	CD4011BKMSR
5962R9662101TCC	<u>3</u> /	CD4011BDTR
5962R9662101TXC	<u>3</u> /	CD4011BKTR
5962R9662101V9A	34371	CD4011BHRSR
5962R9662102VCC	<u>3</u> /	CD4012BDMSR
5962R9662102VXC	<u>3</u> /	CD4012BKMSR
5962R9662102V9A	<u>3</u> /	CD4012BHRSR
5962R9662103VCC	34371	CD4023BDMSR
5962R9662103VXC	34371	CD4023BKMSR
5962R9662103V9A	34371	CD4023BHRSR
5962R9662104VCC	<u>3</u> /	CD4011BDNSR
5962R9662104VXC	<u>3</u> /	CD4011BKNSR
5962R9662104V9A	<u>3</u> /	CD4011BHNSR

STANDARD MICROCIRCUIT DRAWING BULLETIN - Continued.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962R9662105VCC	<u>3/</u>	CD4012BDNSR
5962R9662105VXC	<u>3/</u>	CD4012BKNSR
5962R9662105V9A	<u>3/</u>	CD4012BHNSR
5962R9662106VCC	<u>3/</u>	CD4023BDNSR
5962R9662106VXC	<u>3/</u>	CD4023BKNSR
5962R9662106V9A	<u>3/</u>	CD4023BHNSR

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE  
number

34371

Vendor name  
and address

Intersil Corporation  
2401 Palm Bay Blvd  
PO Box 883  
Melbourne, FL 32902-0883

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.