National Semiconductor

PRELIMINARY

DS1777 TM Bus Transceiver

General Description

The DS1777 is a quad TM (Test and Maintenance) Bus Transceiver. The D to B path is latched. B outputs are open collector with a series Schottky diode, ensuring minimum B output loading. B outputs also have ramped rise and fall times (2.5 ns typical), ensuring minimum TM bus ringing. B inputs have glitch rejection circuitry, 4 ns typical.

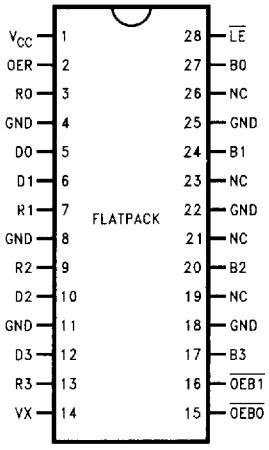
Combining National's patented BTL (Backplane Transceiver Logic) and an advanced BiCMOS process enables the DS1777 to achieve very low power consumption. AC performance is optimized for the TM inter-operability requirements.

The DS1777 is a quad bidirectional transceiver with open collector B and TRI-STATE® R port output drivers. A latch function is provided for the D port signals. The B port output driver is designed to sink 100 mA from 2V and features controlled linear ramp to minimize crosstalk and ringing on the bus.

Features

- Mil-Std-883 qualified
- Low power I_{CCL} = 41 mA max
- B output controlled ramp rate
- B input noise immunity, typically 4 ns
- Separate I/O ports

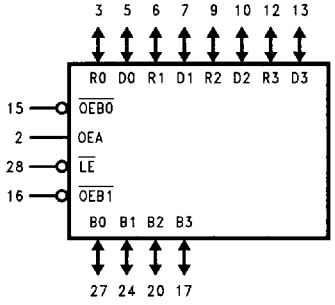
Pin Configuration



TL/F/11882–1

Order Number DS1777W/883
See NS Package WA28D

Logic Symbol



TL/F/11882–2

MIL-STD-883

DEVICE SPECIFICATIONS

Absolute Maximum Ratings (Notes 1 and 2)

The 883 specifications are written to reflect the Rel Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the latest RETS please contact your local National Semiconductor sales office or distributor.

Supply Voltage (V_{CC})	−0.5V to +7.0V
V_X, V_{OH} Output Level Control Voltage (A Outputs)	−0.5V to +7.0V
$\overline{OE}$Bn, OER, $\overline{LE}$ Input Voltage (V_I)	−0.5V to +7.0V
D0−D3, B0−B3 Input Voltage (V_I)	−0.5V to +5.5V
Input Current (I_I)	−40 mA to +5 mA
Voltage Applied to Output in High Output State (V_O)	−0.5V to +V_{CC}V
D0−D3 Current Applied to Output in Low Output State (I_O)	40 mA
B0−B3 Current Applied to Output in Low Output State (I_O)	200 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 10 Sec.)	260°C
ESD Tolerance: C_{ZAP} = 120 pF, R_{ZAP} = 1500Ω	0.5 kV

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Operating Temp. Range (T_A)	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		50	ns

TM Bus Transceiver DS1777

DC Electrical Characteristics V_{CC} = 5V ±10% (Unless Otherwise Specified)

DC testing temp. groups: 1 = +25°C, 2 = +125°C, 3 = −55°C

Symbol	Parameter		Conditions (Notes 3 and 5)		Temp. Group	Min	Typ (Note 4)	Max	Units
V_{IH}	High Level Input Voltage	Except Bn & Rn			1, 2, 3	2			V
		Bn				1.6			V
V_{IL}	Low Level Input Voltage	Except Bn & Rn			1, 2, 3			0.8	V
		Bn						1.45	V
I_{OH}	High Level Output Current	Rn	V_{IN} = V_{IH} V_{OH} = V_{CC} − 2.0V		1, 2, 3			−3	mA
	High Level Output Current	Bn	V_{CC} = Max, OER = $\overline{LE}$ V_{IH} = 2.0V, V_{OH} = 2.1V					100	µA
I_{OL}	Low Level Output Current	Rn	V_{IN} = V_{IL} V_{OL} = 0.5V		1, 2, 3			20	mA
		Bn	V_{OL} = 1.15V					100	mA
I_{OZ}	TRI-STATE Output Leakage Current	Rn Bn			1, 2, 3			±70	µA
V_{OH}	High Level Output Voltage	Rn	V_{CC} = Min, V_{IH} = 1.9V	I_{OH} = −3 mA V_X = V_{CC}	1, 2, 3	2.2		V_{CC}	V
				I_{OH} = −0.4 mA V_X = 3.13V to 3.47V		2.2		V_X	V

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur

Note 2: Unless otherwise specified all voltages are referenced to ground

Note 3: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions. Unless otherwise specified, V_X = V_{CC} for all test conditions.

Note 4: All typical values are at V_{CC} = 5V, T_A = 25°C

Note 5: Due to test equipment limitations, actual test conditions are for V_{IH} = 1.9V and for V_{IL} = 1.2V, however the specified test limits and conditions are guaranteed

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TM Bus Transceiver DS1777 (Continued)

DC Electrical Characteristics V_{CC} = 5V ±10% (Unless Otherwise Specified)

DC testing temp. groups: 1 = +25°C, 2 = +125°C, 3 = −55°C (Continued)

Symbol	Parameter		Conditions (Notes 3 and 5)		Temp. Group	Min	Typ (Note 4)	Max	Units
V_{OL}	Low Output Level Voltage	Rn	V_{CC} = Min, V_{IL} = 1.2V	I_{OL} = 20 mA, $V_X = V_{CC}$				0.5	V
		Bn	V_{CC} = Min, V_{IL} = 0.8V	I_{OL} = 100 mA	1, 2, 3			1.15	V
				I_{OL} = 4 mA		0.4			
V_{IK}	Input Clamp Voltage	Dn	V_{CC} = Min, I_I = −18 mA		1, 2, 3			−1.3	V
		Except Dn & Rn	V_{CC} = Min, I_I = −18 mA					−1.3	V
I_{IH2}	Input Current at Max Input Voltage	$\overline{OEBn}$, OER, $\overline{LE}$	V_{CC} = Min, V_I = 7.0V		1, 2, 3		1	100	μA
		Dn	V_{CC} = Min, V_I = 5.5V				0.01	1	mA
		Bn	V_{CC} = Min, V_I = 5.5V				0.01	1	mA
I_{IH1}	Input Current at Max Input Voltage	$\overline{OEB}$, OER, $\overline{LE}$	V_{CC} = Max, V_I = 2.7V		1, 2, 3			20	μA
		B0–B3	V_{CC} = Max, V_I = 2.1V		1, 2, 3			100	μA
I_{IL}	Low Level Input Current	$\overline{OEB}$, OER, $\overline{LE}$	V_{CC} = Max, V_I = 0.5V		2, 3	−40			μA
					1	−20			μA
		Bn	V_{CC} = Max, V_I = 0.3V		1, 2, 3	−100			μA
I_{OZH} + I_{IH}	TRI-STATE Output Current, High Level Voltage Applied	Rn	V_{CC} = Max, V_O = 2.7V		1, 2, 3			70	μA
I_{OZH} + I_{IL}	TRI-STATE Output Current, Low Level Voltage Applied	Rn	V_{CC} = Max, V_O = 0.5V		1, 2, 3	−70			μA
I_X	High Level Control Current		V_{CC} = Max, $V_X = V_{CC}$, $\overline{LE}$ = OER = $\overline{OEBn}$ = 2.7V, Rn = 2.7V, Bn = 2.0V		1, 2, 3	−100		100	μA
			V_{CC} = Max, V_X = 3.14V & 3.47V, $\overline{LE}$ = OER = $\overline{OEBn}$ = 2.7V, Rn = 2.7V, Bn = 2.0V		1, 2, 3	−10		10	mA
I_{OS}	Short-Circuit Output Current (Note 6)	Rn	V_{CC} = Max, Bn = 1.9V, OER = 2.0V, $\overline{OEBn}$ = 2.7V		1, 2, 3	−60	−75	−150	mA
I_{CC}	Supply Current	I_{CCH}	V_{CC} = Max, V_{IH} (D) = 5.0V		1, 2			37	mA
		I_{CCH}			3			41	mA
		I_{CCL}	V_{CC} = Max, V_{IL}(D) = 0.3V		1, 2, 3			40	mA
		I_{CCZ}	V_{CC} = Max, V_{IL}(D) = 0.3V		1, 2, 3			35	mA
I_{OFF}	Power Off Output Current	Bn	Bn = 2.1V, V_{CC} = 0.0V, V_{IL} = Max or V_{IH} = Min		1, 2, 3			100	μA

Note 6: Not more than one output should be shorted at a time. For testing I_{OS}, the use of high speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

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TM Bus Transceiver DS1777 (Continued)

AC Electrical Characteristics V_{CC} = 5V ± 10% (Unless otherwise specified)

AC testing temp. groups: 1 = +25°C, 2 = +125°C, 3 = −55°C

Symbol	Parameter	Conditions	Temp. Group	Min	Max	Units
B-TO-R PATH						
t_{PLH}	Propagation Delay B to R	Waveform 1, 2	1, 2, 3	4.5	20	ns
t_{PHL}				6	20	ns
t_{PZH}	Output Enable OER to R	Waveform 3, 4	1, 2, 3	4	20	ns
t_{PZL}				4	22	ns
t_{PHZ}	Output Disable OER to R	Waveform 3, 4	1, 2, 3	2	22	ns
t_{PLZ}				2	22	ns
D-TO-B PATH						
t_{PLH}	Propagation Delay D to B	Waveform 1, 2	1, 3 2	2 2	15 25	ns ns
t_{PHL}			1, 3 2	2.5 2.5	13 16	ns ns
t_{PLH}	Propagation Delay $\overline{LE}$ to B	Waveform 1, 2	1, 3 2	2 2	18 30	ns ns
t_{PHL}			1, 3 2	2 2	16 20	ns ns
t_{PLH}	Enable/Disable $\overline{OEBn}$ to B	Waveform 1, 2	1, 3 2	2 2	16 22	ns ns
t_{PHL}			1, 2, 3	3.5	20	ns
t_{TLH}	Transition Time, B Side	1.3V to 1.7V	1, 2, 3	0.5	11	ns
t_{THL}		1.7V to 1.3V	1, 2, 3	0.5	11	ns
SETUP/HOLD/PULSE WIDTH SPECS						
t_S	D to $\overline{LE}$ Setup	Waveform 5	1, 2, 3	7		ns
t_H	D to $\overline{LE}$ Hold	Waveform 5	1, 2, 3	0		ns
t_W	$\overline{LE}$ Pulse Width Low	Waveform 5	1, 2, 3	12		ns

General Description

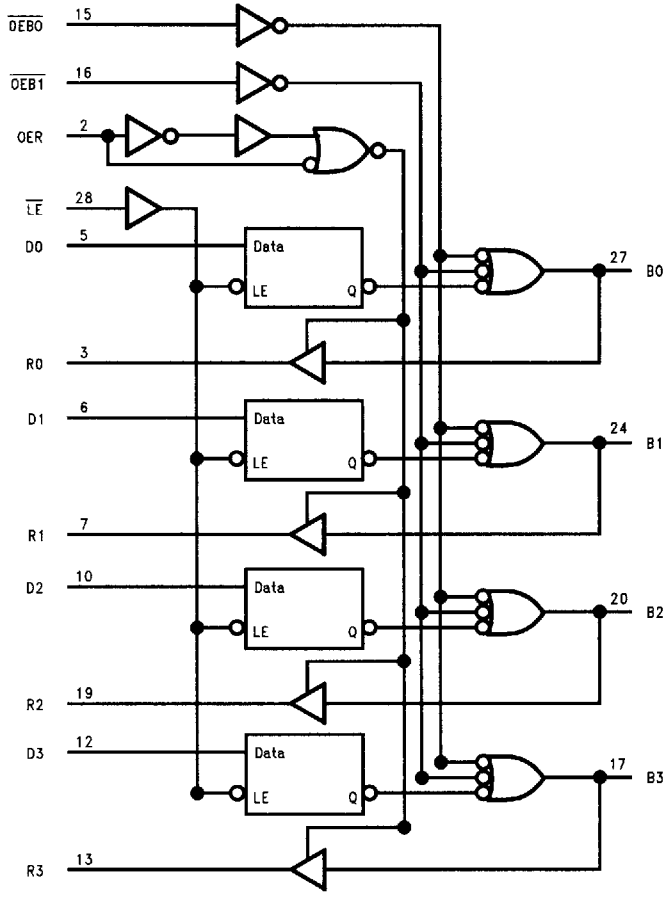
PIN DESCRIPTION

TABLE I. Pin Description

Symbol	Pins	Type	Name and Function
R0	3	O	TTL Level, latched input/TRI-STATE output (with V_X control option)
D0	5	I	
D1	6	I	
R1	7	O	
R2	9	O	
D2	10	I	
D3	12	I	
R3	13	O	
B0	27	I/O	Data input with special threshold circuitry to reject noise/Open Collector output, High current drive
B1	24	I/O	
B2	20	I/O	
B3	17	I/O	
$\overline{OEB0}$	15	I	Enables the B outputs when both pins are low
$\overline{OEB1}$	16	I	
OER	2	I	Enables the R outputs when High
$\overline{LE}$	28	I	Latched when High (a special delay feature is built in for proper enabling times)
V_X	14	I	Clamping voltage keeping V_{OH} from rising above V_X ($V_X = V_{CC}$ for normal use)

General Description (Continued)

FUNCTION DESCRIPTION



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V_{CC} = Pin 1
V_X = Pin 14
GND = Pins 4, 8, 11, 18, 22, 25

FIGURE 1. Functional Logic Diagram

General Description (Continued)

TABLE II. Function Table

Inputs						Latch State	Outputs		Mode
Dn	Bn	$\overline{LE}$	OER	$\overline{OEB0}$	$\overline{OEB1}$		Rn	Bn	
H	X	L	L	L	L	H	Z	H	R TRI-STATE, Data from D to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Qn	Z	Qn	R TRI-STATE, Latched Data to B
H	X	L	H	L	L	H	H	H	Data D to B, B to R
L	X	L	H	L	L	L	L	L	
H	H	H	H	L	L	H	H	Off	Preconditioned Latch Enable
H	L	H	H	L	L	H	L	Off	Data Transfer from B to R
X	X	H	H	L	L	Qn	Qn	Qn	Latch Data D to B, B to R
H	X	L	L	H	X	H	Z	Off	B Off, R TRI-STATE
L	X	L	L	H	X	L	Z	Off	
X	X	H	L	H	X	Qn	Z	Off	
X	H	L	H	H	X	X	H	Off	B Off, Data B to R
X	L	L	H	H	X	X	L	Off	
X	H	H	H	H	X	Qn	H	Off	
X	L	H	H	H	X	Qn	L	Off	
H	X	L	L	X	H	H	Z	Off	B Off, R TRI-STATE
L	X	L	L	X	H	L	Z	Off	
X	X	H	L	X	H	Qn	Z	Off	
X	H	L	H	X	H	X	H	Off	B Off, Data B to R
X	L	L	H	X	H	X	L	Off	
X	H	H	H	X	H	Qn	H	Off	
X	L	H	H	X	H	Qn	L	Off	

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
— = Input not externally driven
Z = High Impedance (off) state
Qn = High or Low Voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition
off = Applies to "B" (OC) outputs only. Indicates that the outputs are turned off.

Note 1: Condition will cause data D to B, B to R

Note 2: The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB0}$ and $\overline{OEB1}$, are Low and $\overline{LE}$ is high.

Note 3: Precaution should be taken to ensure that he B inputs do not float If they do, there are equal to a Low state.

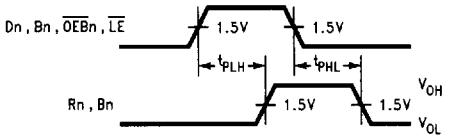
CONTROLLER POWER SEQUENCING OPERATION

The DS1777 has a design feature which controls the output transitions during power up (or down). There are two possible conditions that occur.

1. When $\overline{LE}$ = Low and $\overline{OEB}$n = Low, the B outputs are disabled until the $\overline{LE}$ circuit can take control. This feature ensures that the B outputs will follow the D inputs and allow only one transition during power up (or down).
2. If $\overline{LE}$ = High or $\overline{OEB}$n = High, then the B outputs still remain disabled during power up (or down).

Switching Characteristics

AC WAVEFORMS



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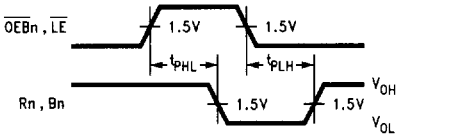
Waveform 1. Propagation Delay for Data to Output



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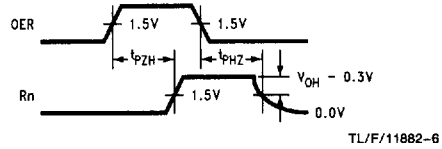
Waveform 2. Propagation Delay for Data to Output



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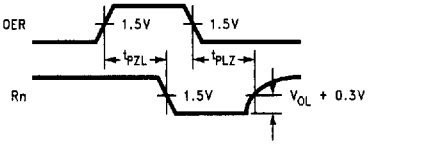
Waveform 3. TRI-STATE Output Enable Time to High Level and Output Disable Time from High Level



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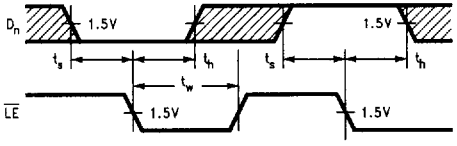
Waveform 4. TRI-STATE Output Enable Time to Low Level and Output Disable Time from Low Level



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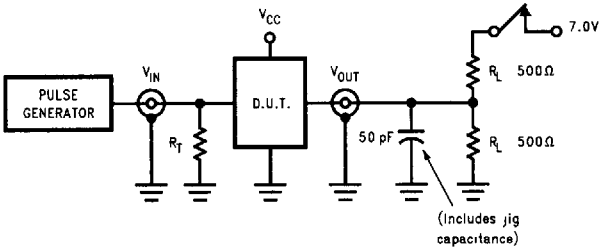
Waveform 5. Data Setup and Hold Times and LE Pulse Widths

The shaded areas indicate when the input is permitted to change for predictable output performance

TEST CIRCUIT AND WAVEFORMS

Test Circuit for TRI-STATE Outputs on A Side



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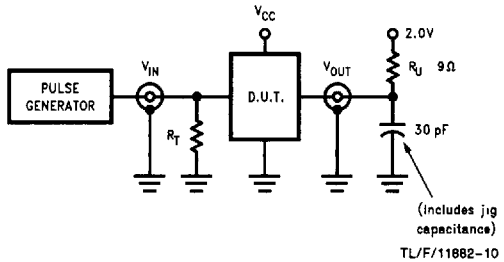
Switch Position

Test	Switch
t_{PLZ}, t_{PZL}	Closed
All Other	Open

Test Circuit for TRI-STATE Outputs on B Side



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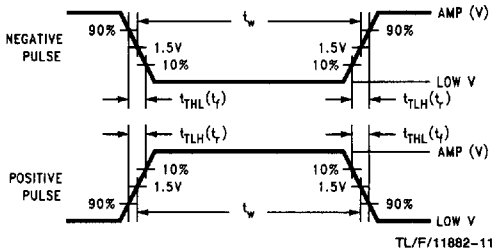
DEFINITIONS

R_L = Load resistor 500Ω
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
R_U = Pull up resistor

Input Pulse Definition



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	Input Pulse Characteristics					
	Amplitude	**Low V**	**Rep. Rate**	**t_W**	**t_{TLH}**	**t_{THL}**
D Side	3.0V	0.0V	1 MHz	500 ns	2 ns	2 ns
B Side	2.0V	1.0V	1 MHz	500 ns	2 ns	2 ns

National Semiconductor

Ordering Information and Physical Dimensions

Ordering Information

SCAN 18 245 T SS C X

- SCAN — Serially Controlled Access Network
- 18 — 18-bit Logic
- 245 — Function Type
- T — Technology Designator
  - T = TTL input, TTL output CMOS device
  - C = CMOS input/output CMOS device
  - B = Bipolar TTL device
  - E = ECL device
  - A = BiCMOS device
  - F = TTL input/CMOS output CMOS device
- SS — Package Code
  - SS = 25 mil pitch (JEDEC) SSOP
  - F = 25 mil pitch Ceramic Flatpak
  - D = Ceramic DIP
  - L = Leadless Chip Carrier (LCC)
- C — Temperature Range
  - C = Commercial (−40°C to +85°C)
  - M = Military (−55°C to +125°C)
- X — Special Variations
  - X = Tape and Reel
  - QB = Military grade device with environmental and burn-in processing

SCAN PSC100 F XXXX

- SCAN — Serially Controlled Access Network
- PSC100 — Part Number
  - PSC100 = Protocol Converter
  - PSC110 = SCAN Bridge
- F — Technology Designator
  - T = TTL input/TTL output CMOS device
  - C = CMOS input/output CMOS device
  - B = Bipolar TTL device
  - E = ECL device
  - A = BiCMOS device
  - F = TTL input/CMOS output CMOS device
- XXXX — Package/Temp Designator
  - SC = 50 mL Pitch (JEDEC) SOIC Temperature Range −40°C to +85°C
  - DMQB = Ceramic DIP, Military Temperature Range, 883 Processing
  - LMQB = Leadless Chip Carrier, Military Temperature Range, 883 Processing

SSOP Package Thermal Information

THERMAL RESISTANCE FOR SSOP PACKAGES

Package	Paddle Dimensions (mils)	θ_{JA} 0 LFPM (°C/W)	θ_{JA} 225 LFPM (°C/W)	θ_{JA} 500 LFPM (°C/W)	θ_{JA} 900 LFPM (°C/W)	θ_{JC}
20LD SSOP	110 x 144	127.0	99.4	90.1	78.5	N/A
24LD SSOP	98 x 106	117.0	91.4	82.7	73.5	N/A
24LD SSOP	120 x 150	100.8	81.3	72.1	65.7	25.7
48LD SSOP	190 x 190	75.5	58.0	51.5	44.0	21.5
56LD SSOP	190 x 190	67.8	53.0	47.4	42.1	18.5

THERMAL RESISTANCES FOR THE FLATPAK PACKAGES

Package	Cavity Dimensions (mils)	θ_{JA} 0 LFPM (°C/W)	θ_{JA} 225 LFPM (°C/W)	θ_{JA} 500 LFPM (°C/W)	θ_{JA} 900 LFPM (°C/W)	θ_{JC}
48LD FP	250 x 250	74.4	58.1	50.0	43.9	6.6
56LD FP	250 x 250	59.8	47.9	39.0	35.1	3.4

Dry Pack

Dry Pack is moisture proof packing that is used to store SSOP devices to reduce the susceptibility of the "popcorn effect". Humidity collects inside the package by seeping through the plastic. If moisture is inside the device when the unit goes through a solder machine, the heat quickly changes the moisture to steam, and the pressurized steam pops open the package . . . thus the popcorn effect.

The Dry Pack bag is hermetically sealed and contains a small bag of desiccant which further helps to reduce moisture. All of the SCAN 56-pin SSOP devices will be shipped in Dry Pack bags. Included with the devices will be the following warning label and instructions for rebake:

Dry Pack Warning Label for Surface Mount Packages

National Semiconductor

ELECTROSTATIC SENSITIVE DEVICES
Require Proper Handling Procedures

CAUTION
This Bag Contains
MOISTURE SENSITIVE DEVICES

1. Shelf life in sealed bag: 24 months at <40°C and <90% Relative Humidity (RH).
2. Upon opening this bag, devices to be subjected to I.R., V.P.R. or equivalent process must be:
   a. Mounted within 48 hours at factory conditions of <30°C/60% RH, or
   b. Stored at <10% RH.
3. Devices require baking, before mounting, if:
   a. Humidity Indicator Card is >20% when read at 23°C ±5°C.
   b. 2a or 2b are not met.
4. If baking is required, devices may be baked for:
   a. 19 hours at 40°C +5°C/−0°C and <5% RH for low temperature device containers, or
   b. 8 hours at 125°C ±5°C for high temperature device containers.

Dry-Pack Seal Date: _____
(IF BLANK, SEE BAR CODE LABEL)

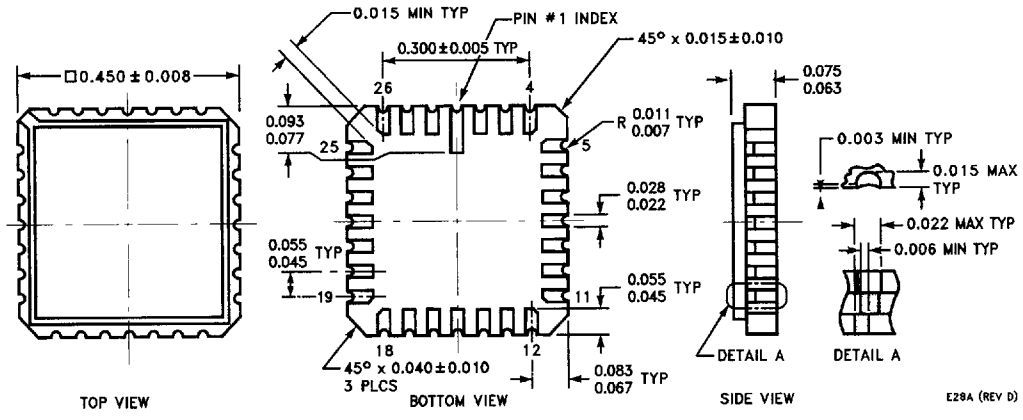
BAG SN 045317 MFR LOT No. C32729

Please follow these instructions carefully to avoid the popcorn effect.

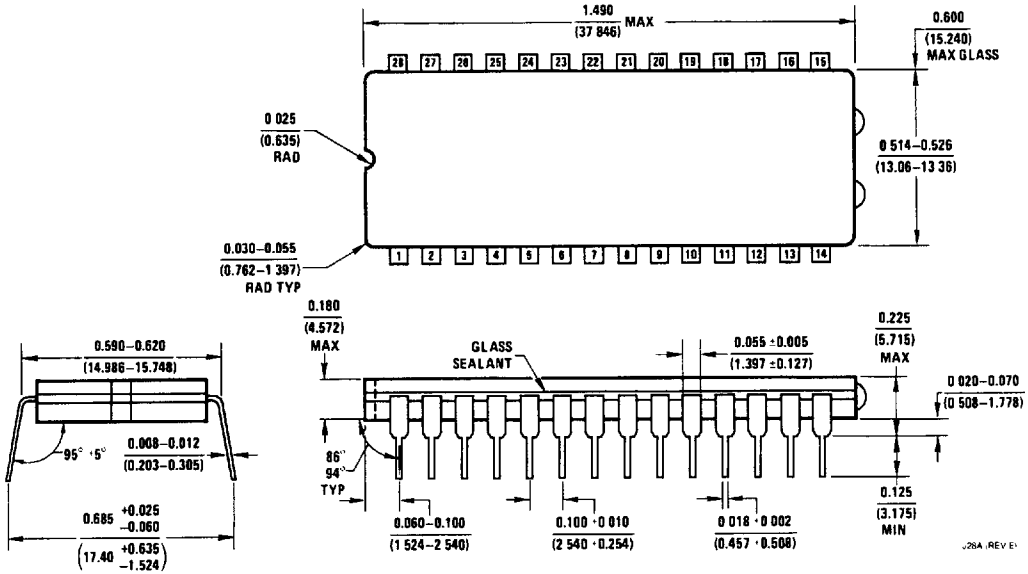
National Semiconductor

All dimensions are in inches (millimeters)

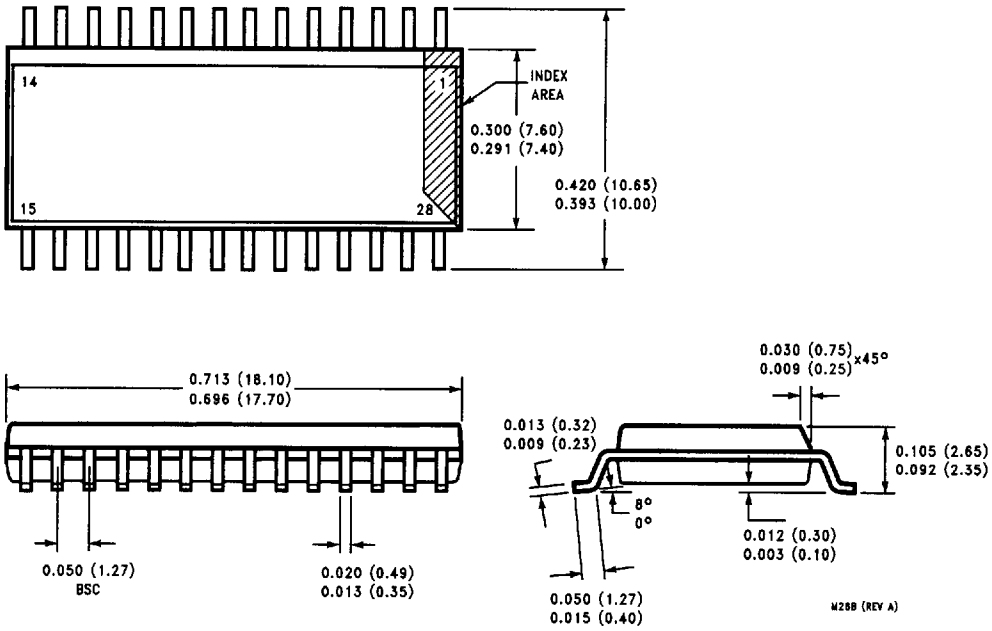
28 Lead Ceramic Leadless Chip Carrier, Type C
NS Package Number E28A



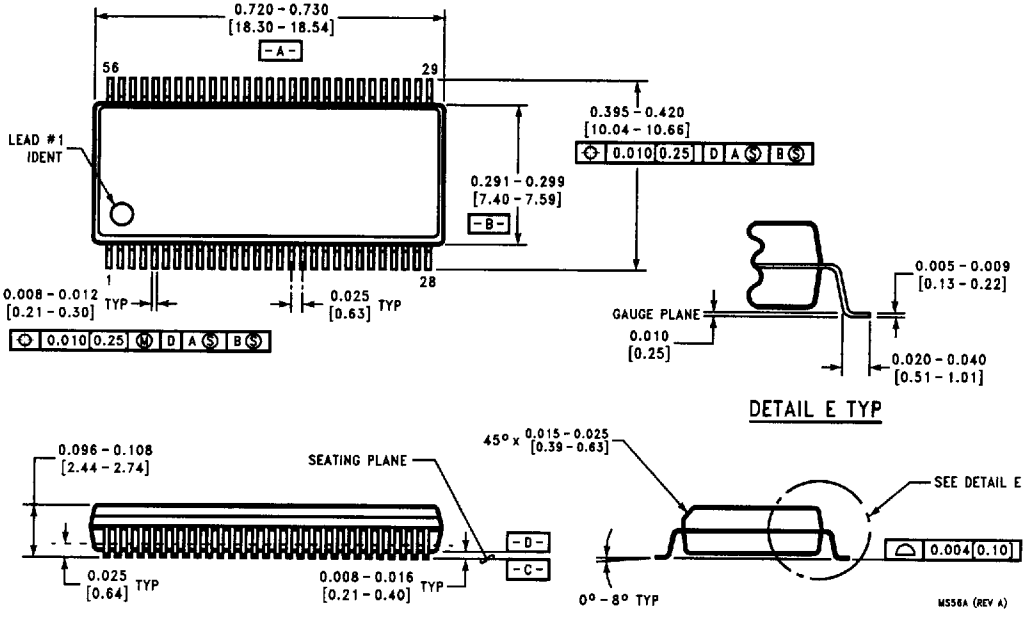
28 Lead Ceramic Dual-in-Line Package
NS Package Number J28A



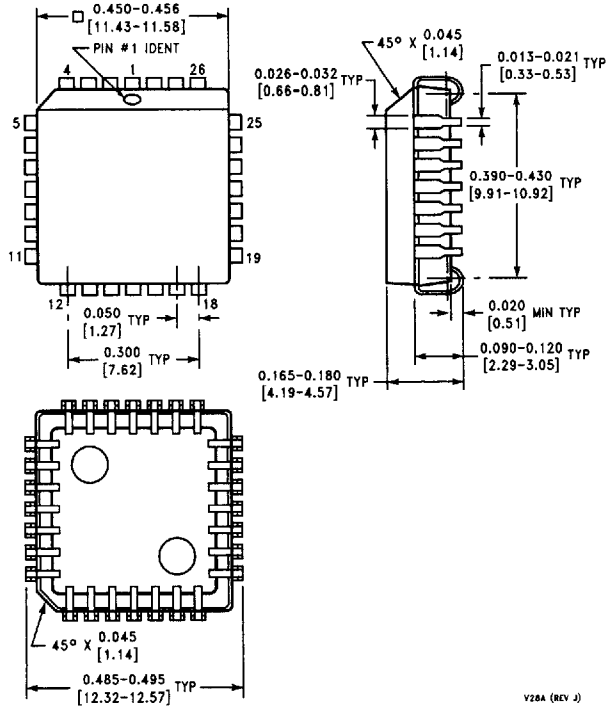
28 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M28B



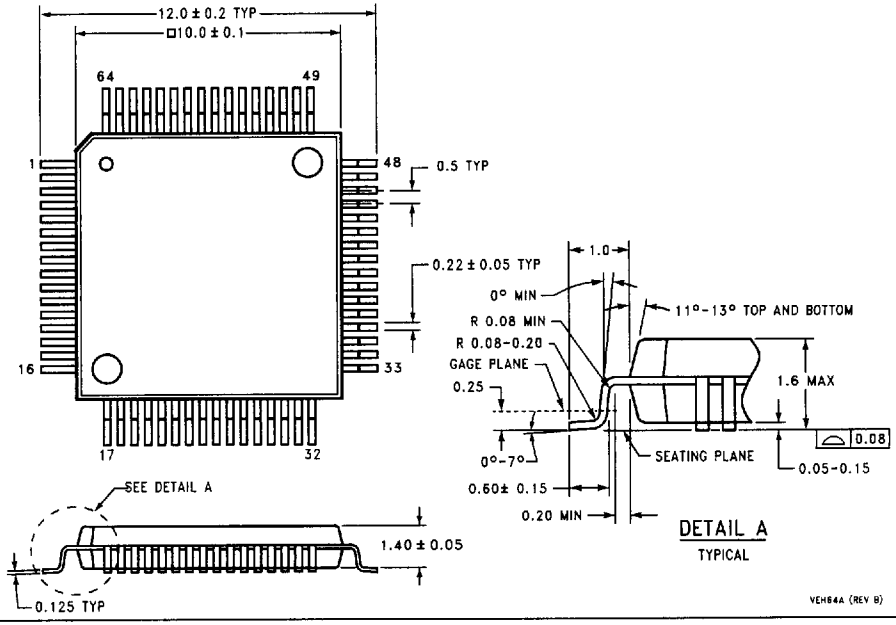
56 Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC
NS Package Number MS56A



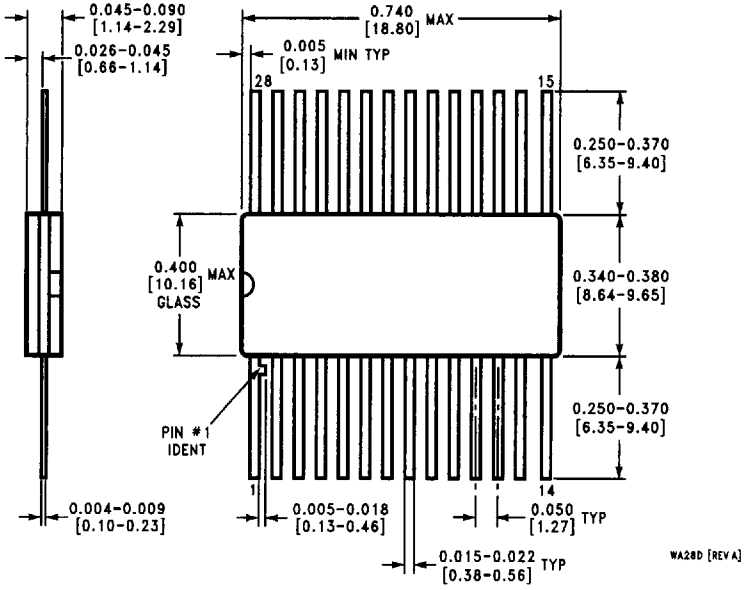
28 Lead Molded Plastic Leaded Chip Carrier
NS Package Number V28A



64 Lead (10mm x 10mm) Molded Plastic Quad Flat Package, JEDEC
NS Package Number VEH64A



28 Lead Cerpack
NS Package Number WA28D



56 Lead Ceramic Flatpack
NS Package Number WA56A