

DATA SHEET

74LV10

Triple 3-input NAND gate

Product specification

1997 Feb 12

IC24 Data Handbook

Triple 3-input NAND gate

74LV10

FEATURES

- Wide operating voltage 1.0 to 5.5 V
- Optimized for Low Voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7\text{ V}$ and $V_{CC} = 3.6\text{ V}$
- Typical V_{OLP} (output ground bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_{amb} = 25^\circ\text{C}$.
- Typical V_{OHV} (output V_{OH} undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_{amb} = 25^\circ\text{C}$.
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV10 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT10.

The 74LV10 provides the 3-input NAND function.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f \leq 2.5\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB, nC to nY	$C_L = 15\text{ pF}$; $V_{CC} = 3.3\text{ V}$	9	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	See Notes 1 and 2	12	pF

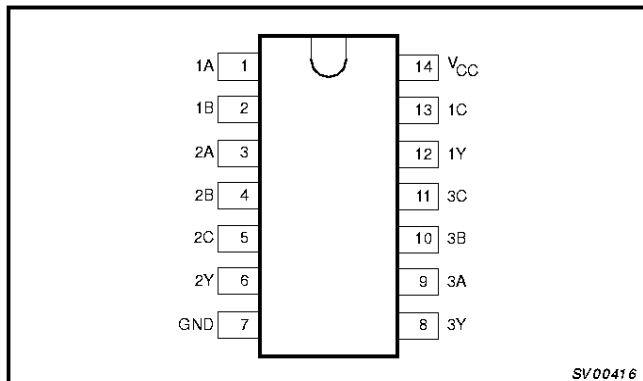
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_I = \text{GND}$ to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	-40°C to $+125^\circ\text{C}$	74LV10 N	74LV10 N	SOT27-1
14-Pin Plastic SO	-40°C to $+125^\circ\text{C}$	74LV10 D	74LV10 D	SOT108-1
14-Pin Plastic SSOP Type II	-40°C to $+125^\circ\text{C}$	74LV10 DB	74LV10 DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40°C to $+125^\circ\text{C}$	74LV10 PW	74LV10PW DH	SOT402-1

PIN CONFIGURATION



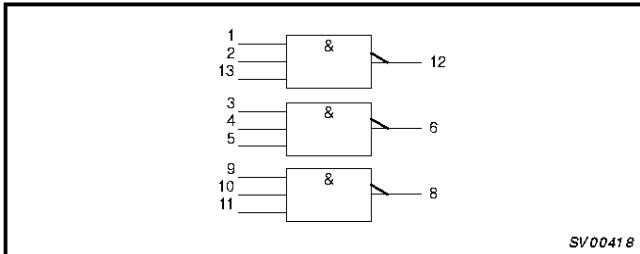
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A – 3A	Data inputs
2, 4, 10	1B – 3B	Data inputs
7	GND	Ground (0 V)
12, 6, 8	1Y – 3Y	Data outputs
13, 5, 11	1C – 3C	Data inputs
14	V_{CC}	Positive supply voltage

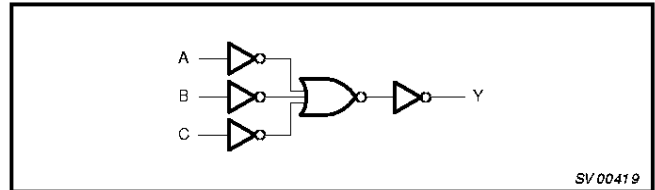
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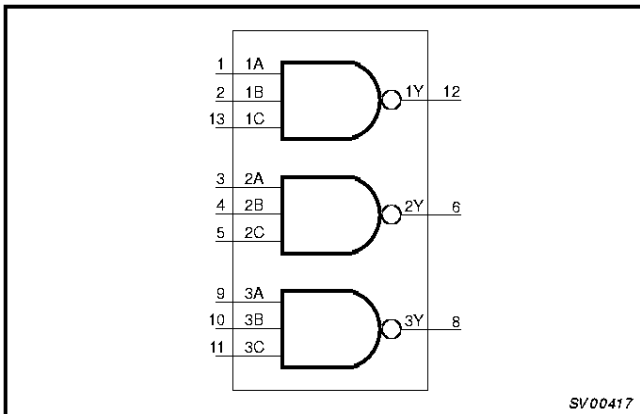
LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (ONE GATE)



LOGIC SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

NOTES:

H = HIGH voltage level
L = LOW voltage level

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note ¹	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics per device	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$ $V_{CC} = 3.6V$ to $5.5V$	– – – –	– – – –	500 200 100 50	ns/V

NOTE:

1. The LV is guaranteed to function down to $V_{CC} = 1.0V$ (input levels GND or V_{CC}); DC characteristics are guaranteed from $V_{CC} = 1.2V$ to $V_{CC} = 5.5V$.

ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25 35	mA
$\pm I_{GND},$ $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs – bus driver outputs		50 70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP ¹	MAX	MIN	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	V _{CC}	0.6		V _{CC}		V
		V _{CC} = 2.0V	1.4			1.4		
		V _{CC} = 2.7 to 3.6V	2.0			2.0		
		V _{CC} = 4.5 to 5.5V	0.7 * V _{CC}			0.7 * V _{CC}		
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V		0.4	GND		GND	V
		V _{CC} = 2.0V			0.6		0.6	
		V _{CC} = 2.7 to 3.6V			0.8		0.8	
		V _{CC} = 4.5 to 5.5			0.3 * V _{CC}		0.3 * V _{CC}	
V _{OH}	HIGH level output voltage; all outputs	V _{CC} = 1.2V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA		1.2				V
		V _{CC} = 2.0V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	1.8	2.0		1.8		
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	2.5	2.7		2.5		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	2.8	3.0		2.8		
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	4.3	4.5		4.3		
V _{OH}	HIGH level output voltage; STANDARD outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 6mA	2.40	2.82		2.20		V
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; -I _O = 12mA	3.60	4.20		3.50		
V _{OH}	HIGH level output voltage; BUS driver outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 8mA	2.40	2.82		2.20		V
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; -I _O = 16mA	3.60	4.20		3.50		
V _{OL}	LOW level output voltage; all outputs	V _{CC} = 1.2V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0				V
		V _{CC} = 2.0V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
V _{OL}	LOW level output voltage; STANDARD outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 6mA		0.25	0.40		0.50	V
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; I _O = 12mA		0.35	0.55		0.65	
V _{OL}	LOW level output voltage; BUS driver outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 8mA		0.20	0.40		0.50	V
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; I _O = 16mA		0.35	0.55		0.65	
I _I	Input leakage current	V _{CC} = 5.5V; V _I = V _{CC} or GND			1.0		1.0	µA
I _{oz}	3-State output OFF-state current	V _{CC} = 5.5V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND			5		10	µA
I _{CC}	Quiescent supply current; SSI	V _{CC} = 5.5V; V _I = V _{CC} or GND; I _O = 0			20.0		40	µA
	Quiescent supply current; flip-flops	V _{CC} = 5.5V; V _I = V _{CC} or GND; I _O = 0			20.0		80	
I _{CC}	Quiescent supply current; MSI	V _{CC} = 5.5V; V _I = V _{CC} or GND; I _O = 0			20.0		160	µA
	Quiescent supply current; LSI	V _{CC} = 5.5V; V _I = V _{CC} or GND; I _O = 0			500		1000	
ΔI _{CC}	Additional quiescent supply current	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V			500		850	µA

NOTE:1. All typical values are measured at T_{amb} = 25°C.

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AC CHARACTERISTICS

GND = 0V; $t_r = t_f = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				-40 to +85 °C			-40 to +125 °C		
				$V_{CC}(\text{V})$	MIN	TYP ¹	MAX	MIN	
t_{PHL}/t_{PLH}	Propagation delay nA, nB, nC to nY	Figure 1, 2	1.2		55				ns
			2.0		19	36		44	
			2.7		15	26		33	
			3.0 to 3.6		10 ²	21		26	
			4.5 to 5.5						

NOTES:

- Unless otherwise stated, all typical values are measured at $T_{amb} = 25^\circ\text{C}$.
- Typical values are measured at $V_{CC} = 3.3\text{V}$.

AC WAVEFORMS

$V_M = 1.5\text{V}$ at $V_{CC} \geq 2.7\text{V}$;
 $V_M = 0.5 \times V_{CC}$ at $< 2.7\text{V}$ and $\geq 4.5\text{V}$;
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

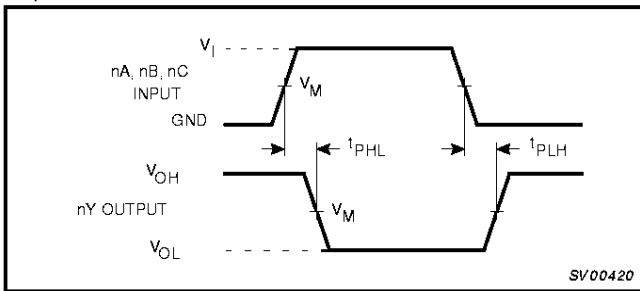


Figure 1. Input (nA, nB, nC) to output (nY) propagation delays.

TEST CIRCUIT

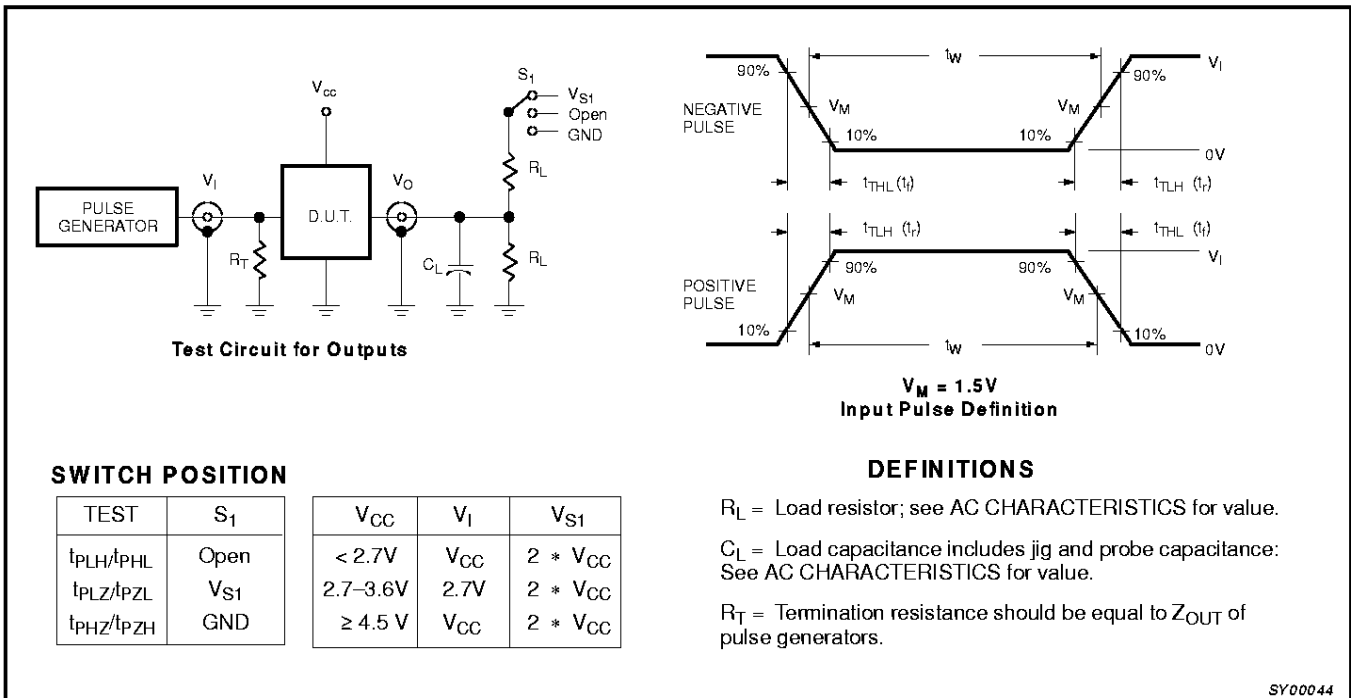


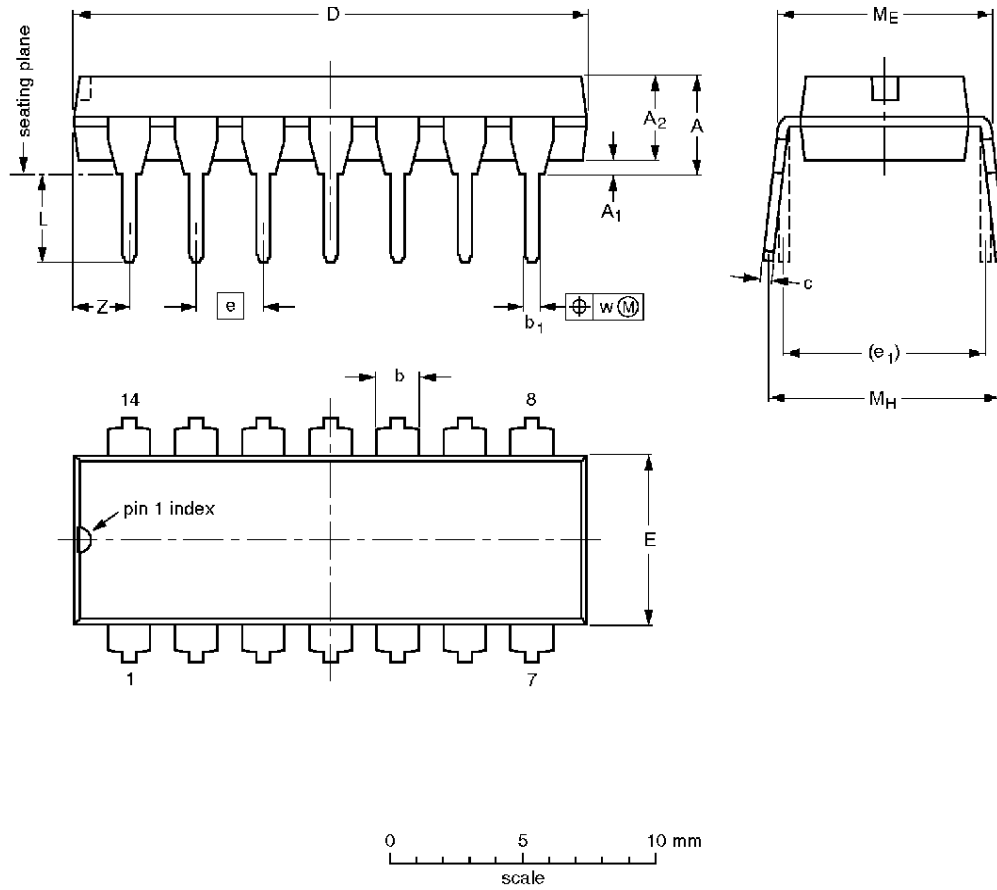
Figure 2. Load circuitry for switching times.

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

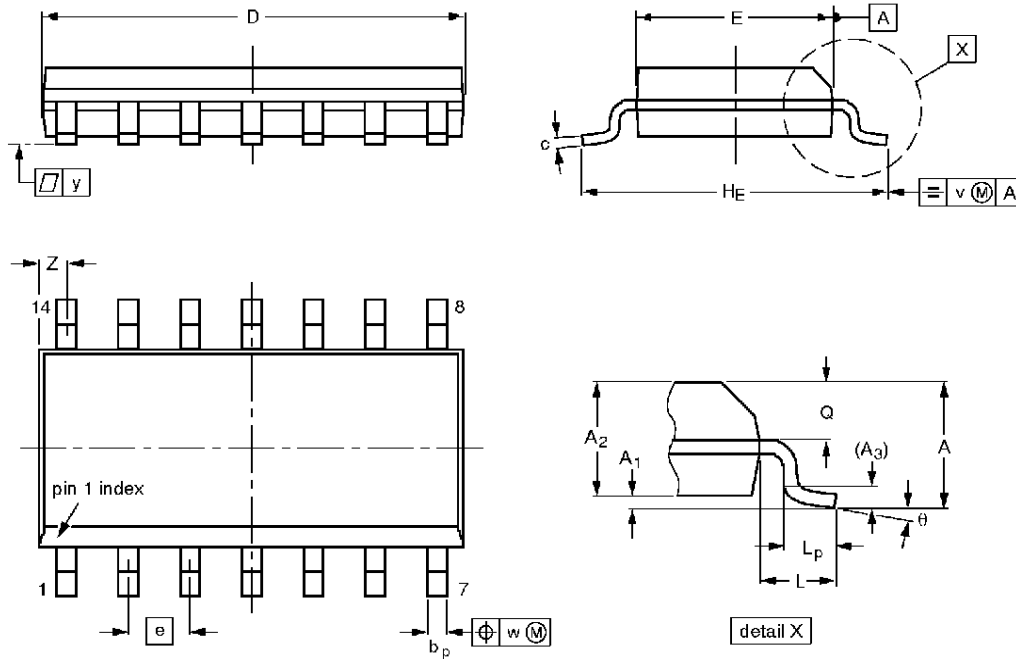
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				92-11-17 95-03-11

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

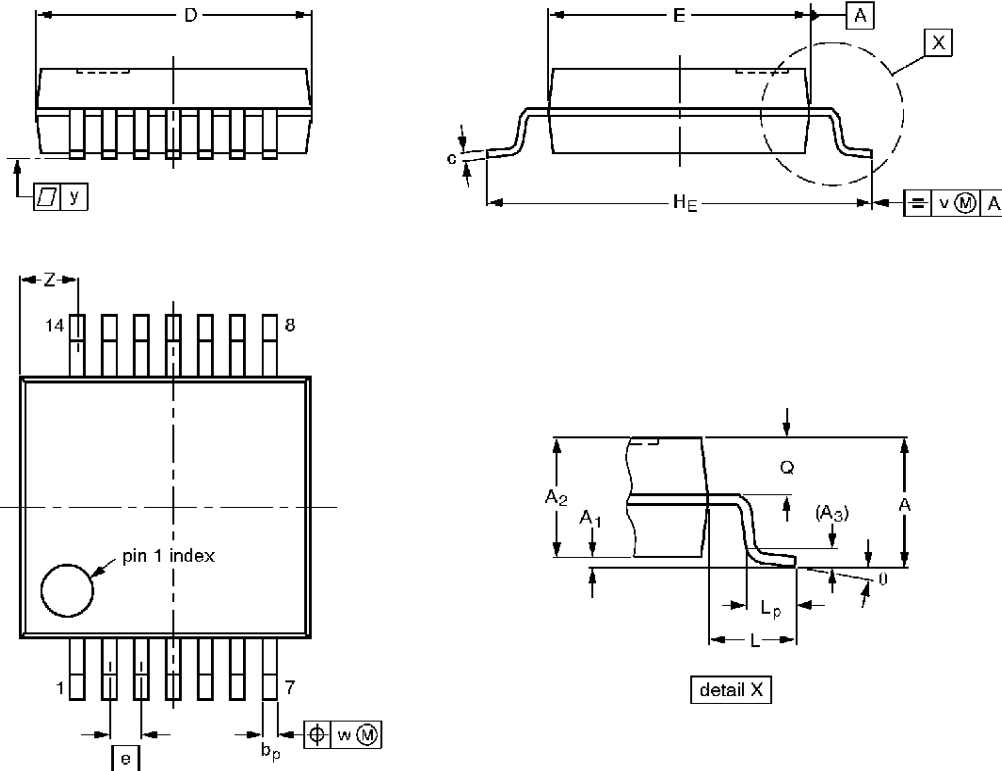
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				91-08-10 95-01-23

Triple 3-input NAND gate

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

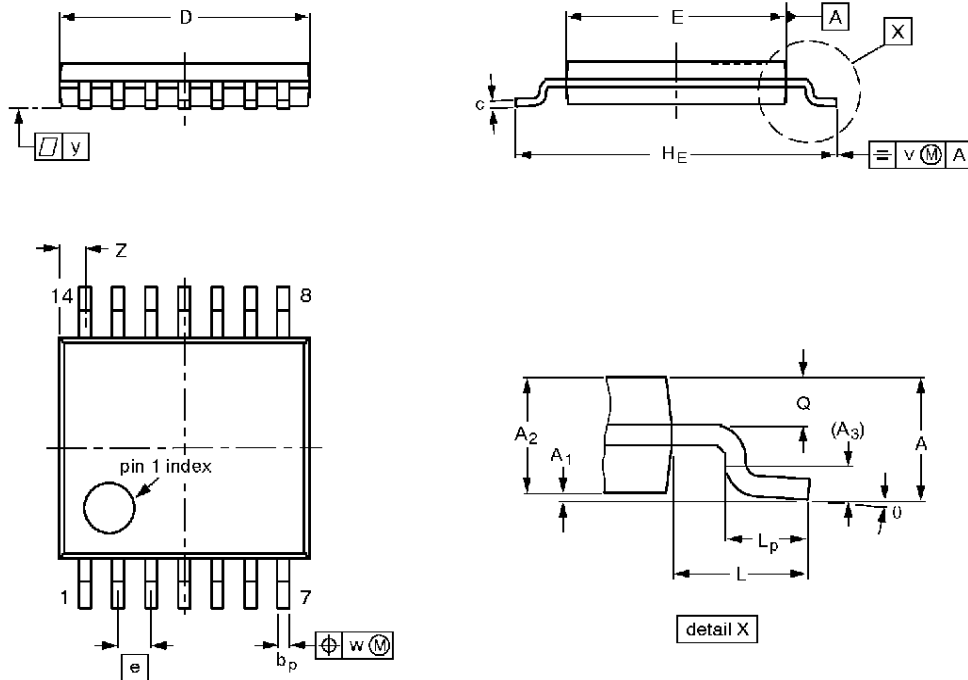
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT337-1		MO-150AB			95-02-04 96-01-18

Triple 3-input NAND gate

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				94-07-12 95-04-04

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NOTES

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DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or In Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
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