FAST CMOS 12-BIT TRI-PORT BUS EXCHANGER

IDT54/74FCT162260AT/CT

FEATURES:

- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{SK(o)}$ (Output Skew) < 250ps
- Low input and output leakage ≤1µA (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- V_{CC} = 5V ±10%
- Balanced Output Drivers:
  - ±24mA (industrial)
  - ±16mA (military)
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C
- Available in the following packages:
  - Industrial: SSOP, TSSOP, TVSOP
  - Military: CERPACK

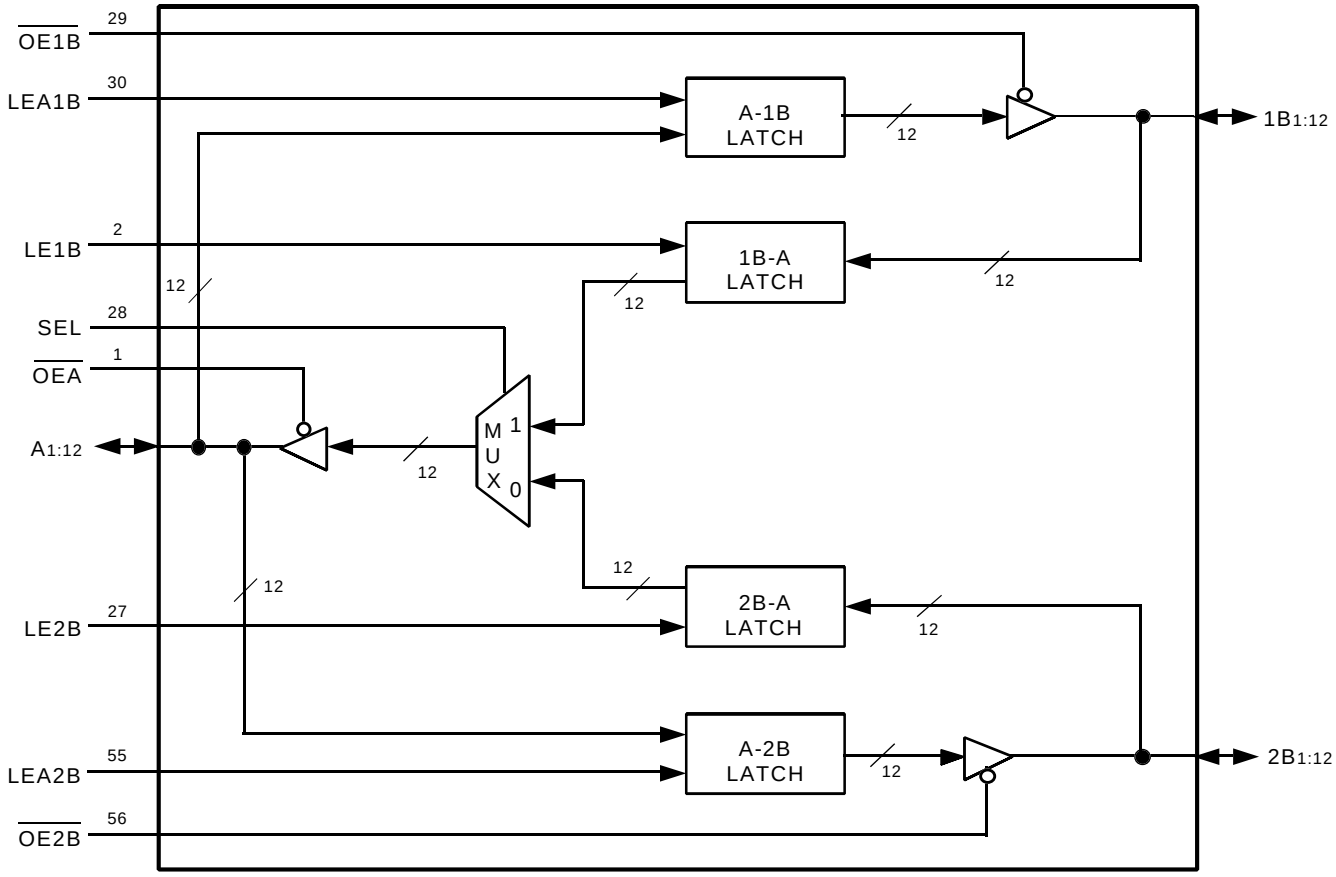
DESCRIPTION:

The FCT162260T Tri-Port Bus Exchangers are high-speed 12-bit latched bus multiplexers/transceivers for use in high-speed microprocessor applications. These Bus Exchangers support memory interleaving with latched outputs on the B ports and address multiplexing with latched inputs on the B ports.

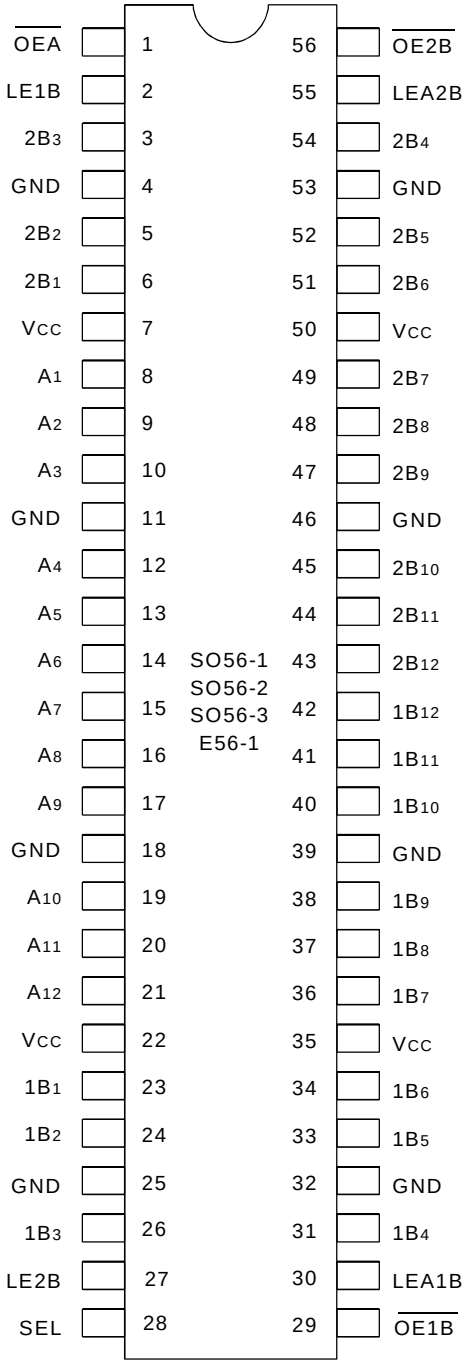
The Tri-Port Bus Exchanger has three 12-bit ports. Data may be transferred between the A port and either/both of the B ports. The latch enable (LE1B, LE2B, LEA1B and LEA2B) inputs control data storage. When a latch-enable input is high, the latch is transparent. When a latch-enable input is low, the data at the input is latched and remains latched until the latch enable input is returned high. Independent output enables ($\overline{OE1B}$ and $\overline{OE2B}$) allow reading from one port while writing to the other port.

The FCT162260T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times - reducing the need for external series terminating resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP/ CERPACK
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXX Output and I/O terminals.
3. Output and I/O terminals for FCT162XXX.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Signal	I/O	Description
A(1:12)	I/O	Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus.
1B(1:12)	I/O	Bidirectional Data Port 1B. Connected to the even path or even bank of memory.
2B(1:12)	I/O	Bidirectional Data Port 2B. Connected to the odd path or odd bank of memory.
LEA1B	I	Latch Enable Input for A-1B Latch. The Latch is open when LEA1B is HIGH. Data from the A-port is latched on the HIGH to LOW transition of LEA1B.
LEA2B	I	Latch Enable Input for A-2B Latch. The Latch is open when LEA2B is HIGH. Data from the A-Port is latched on the HIGH to LOW transition of LEA2B.
LE1B	I	Latch Enable Input for the 1B-A Latch. The Latch is open when LE1B is HIGH. Data from the 1B port is latched on the HIGH to LOW transition of LE1B.
LE2B	I	Latch Enable Input for the 2B-A Latch. The Latch is open when LE2B is HIGH. Data from the 2B port is latched on the HIGH to LOW transition of LE2B.
SEL	I	1B or 2B Path Selection. When HIGH, SEL enables data transfer from 1B Port to A Port. When LOW, SEL enables data transfer from 2B Port to A Port.
$\overline{OEA}$	I	Output Enable for A Port (Active LOW).
$\overline{OE1B}$	I	Output Enable for 1B Port (Active LOW).
$\overline{OE2B}$	I	Output Enable for 2B Port (Active LOW).

FUNCTION TABLES(1)

Inputs						Output
1B	2B	SEL	LE1B	LE2B	$\overline{OEA}$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A(1)
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A(1)
X	X	X	X	X	H	Z

Inputs					Outputs	
A	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	B(1)
L	H	L	L	L	L	B(1)
H	L	H	L	L	B(1)	H
L	L	H	L	L	B(1)	L
X	L	L	L	L	B(1)	B(1)
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

NOTES:
1. Output level before the indicated steady-state input conditions were established.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = -40°C to +85°C, V_{CC} = 5.0V ±10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	5	500	µA

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OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL I_{OH} = –24mA IND.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL I_{OL} = 24mA IND.	—	0.3	0.55	V

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NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ±5µA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Output Port Enabled LExx = V_{CC} One Input Bit Toggling One Output Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
		50% Duty Cycle One Output Port Enabled LExx = V_{CC} One Input Bit Toggling One Output Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	1.8	3.5[5]	
		50% Duty Cycle One Output Port Enabled LExx = V_{CC} Twelve Input Bits Toggling Twelve Output Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	4.8	12.5[5]	

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

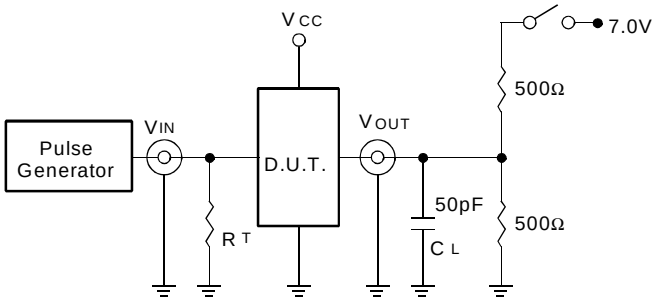
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT162260AT				FCT162260CT				FCT162260ET				Unit
			Ind.		Mil.		Ind.		Mil.		Ind.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Ax to 1Bx or Ax to 2Bx	C_L = 50pF R_L = 500Ω	1.5	5.2	1.5	5.6	1.5	4.7	1.5	5.1	1.5	3.6	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay 1Bx to Ax or 2Bx to Ax		1.5	5.6	1.5	5.9	1.5	5	1.5	5.4	1.5	3.6	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay LExB to Ax		1.5	5.2	1.5	5.6	1.5	4.7	1.5	5.1	1.5	4	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay LEA1B to 1Bx or LEA2B to 2Bx		1.5	4.7	1.5	5.2	1.5	4.4	1.5	4.8	1.5	4	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay SEL to Ax		1.5	5.2	1.5	5.6	1.5	4.7	1.5	5.1	1.5	4	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ to Ax, $\overline{OE1B}$ to 1BX, or $\overline{OE2B}$ to 2Bx		1.5	5.7	1.5	6.1	1.5	5.1	1.5	5.4	1.5	4.4	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ to Ax, $\overline{OE1B}$ to 1BX, or $\overline{OE2B}$ to 2Bx		1.5	4.4	1.5	4.8	1.5	4	1.5	4.4	1.5	4	—	—	ns
t_{SU}	Set-Up Time, HIGH or LOW Data to Latch		1.5	—	1.5	—	1	—	1	—	1	—	—	—	ns
t_H	Hold Time, Latch to Data		1	—	1.5	—	1	—	1.5	—	1	—	—	—	ns
t_W	Pulse Width, Latch HIGH[4]		3	—	3	—	3	—	3	—	3	—	—	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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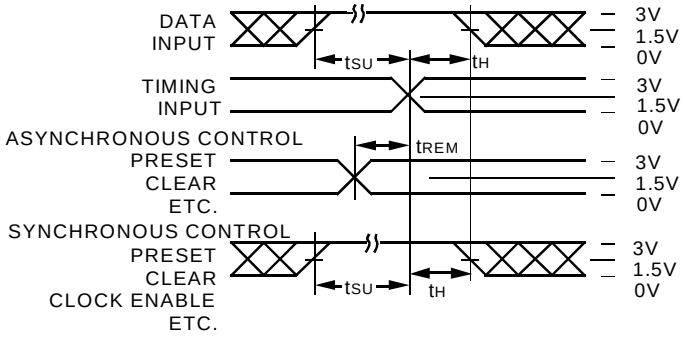
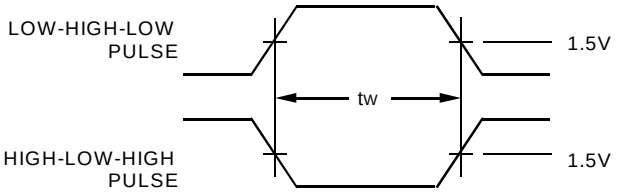
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

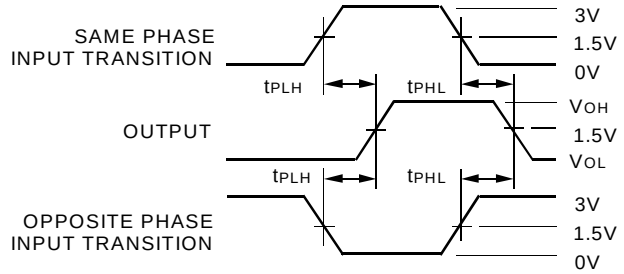
SET-UP, HOLD, AND RELEASE TIMES



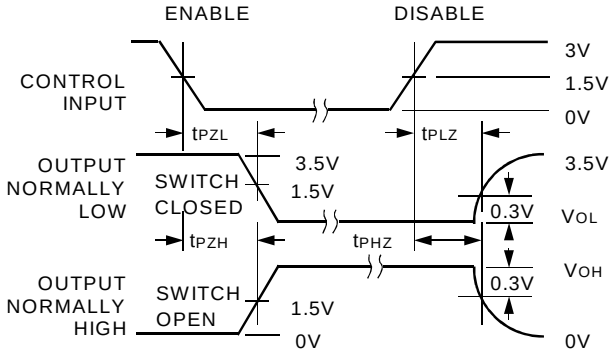
PULSE WIDTH



PROPAGATION DELAY



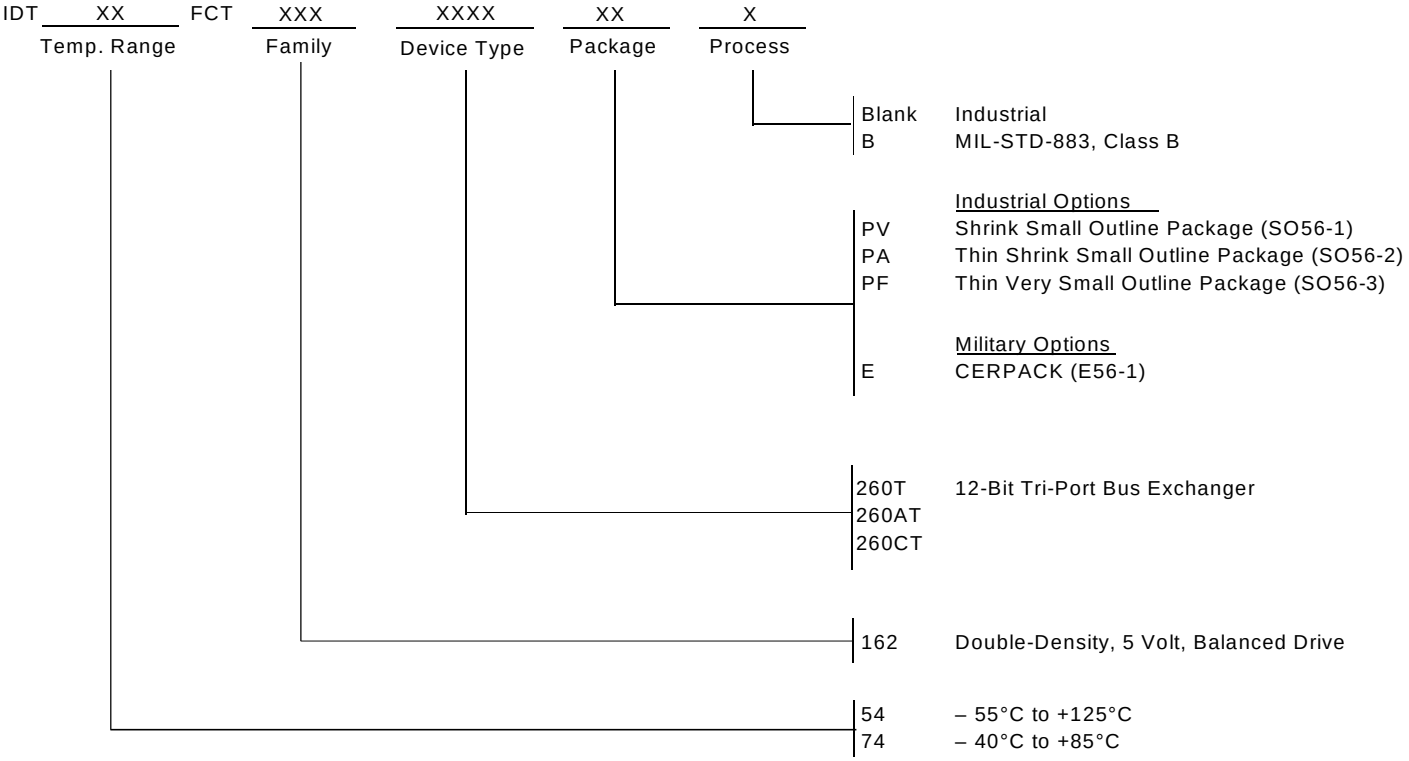
ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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