- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Support Live Insertion**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs**

SN54LVT125 . . . J PACKAGE
SN74LVT125 . . . D, DB, OR PW PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	14	V_{CC}
1A	2	13	4$\overline{OE}$
1Y	3	12	4A
2$\overline{OE}$	4	11	4Y
2A	5	10	3$\overline{OE}$
2Y	6	9	3A
GND	7	8	3Y
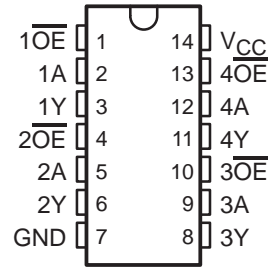
SN54LVT125 . . . FK PACKAGE
(TOP VIEW)
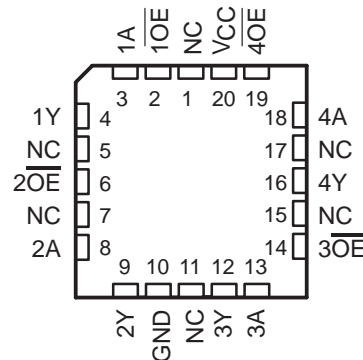
NC – No internal connection

description

These bus buffers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The ′LVT125 feature independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable ($\overline{OE}$) input is high.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT125 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT125 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT125 is characterized for operation from −40°C to 85°C.

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FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol[†]
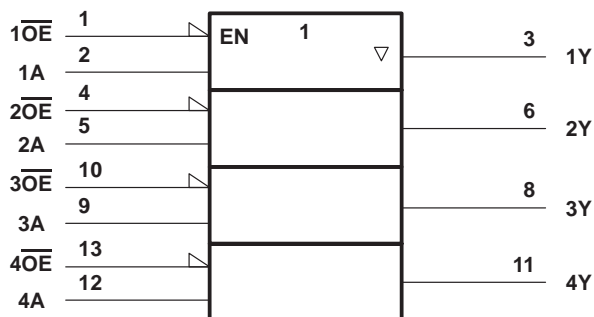
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984
and IEC Publication 617-12.

logic diagram (positive logic)
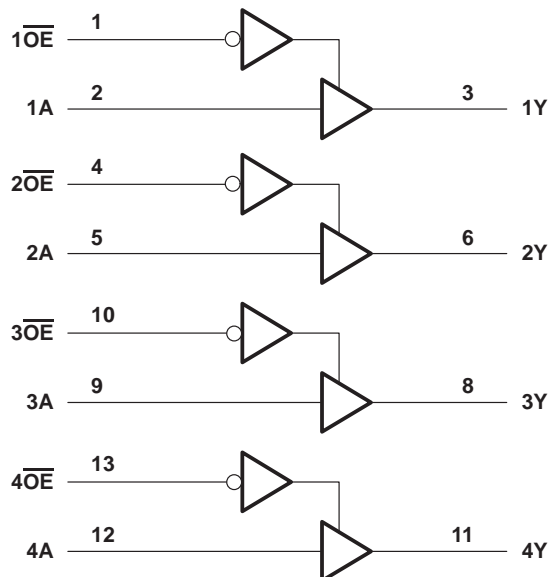
Pin numbers shown are for the D, DB, J, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	−0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT125	96 mA
SN74LVT125	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT125	48 mA
SN74LVT125	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 3): D package	1.25 W
DB or PW package	0.5 W
Storage temperature range, T_{stg}	−65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LVT125 MIN	SN54LVT125 MAX	SN74LVT125 MIN	SN74LVT125 MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4:   Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT125 MIN	SN54LVT125 TYP†	SN54LVT125 MAX	SN74LVT125 MIN	SN74LVT125 TYP†	SN74LVT125 MAX	UNIT
V_{IK}	V_{CC} = 2.7 V, $\quad$ I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡, $\quad I_{OH}$ = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V, $\quad$ I_{OH} = −8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = −24 mA	2						
		I_{OH} = −32 mA				2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2			0.2	V
		I_{OL} = 24 mA			0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA			0.4			0.4	
		I_{OL} = 32 mA			0.5			0.5	
		I_{OL} = 48 mA			0.55				
		I_{OL} = 64 mA						0.55	
I_I	V_{CC} = 0 or MAX‡, $\quad V_I$ = 5.5 V				10			10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND $\quad$ Control inputs			±1			±1	
		V_I = V_{CC} $\quad$ Data inputs			1			1	
		V_I = 0 $\quad$ Data inputs			−5			−5	
I_{off}	V_{CC} = 0, $\quad$ V_I or V_O = 0 to 4.5 V				±100			±100	µA
$I_{I(hold)}$	V_{CC} = 3 V $\quad$ Data inputs	V_I = 0.8 V	75			75			µA
		V_I = 2 V	−75			−75			
I_{OZH}	V_{CC} = 3.6 V, $\quad$ V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V, $\quad$ V_O = 0.5 V				−5			−5	µA
I_{CC}	V_{CC} = 3.6 V, $\quad$ I_O = 0, $\quad V_I$ = V_{CC} or GND	Outputs high		0.12	0.19		0.12	0.19	mA
		Outputs low		4.5	7		4.5	7	
		Outputs disabled		0.12	0.19		0.12	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, $\quad$ One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				0.3			0.2	mA
C_i	V_I = 3 V or 0			4			4		pF
C_o	V_O = 3 V or 0			8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

TEXAS INSTRUMENTS

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT125				SN74LVT125					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	A	Y	1	4.2		4.7	1	2.7	4		4.5	ns
t_{PHL}			1	4.1		5.1	1	2.9	3.9		4.9	
t_{PZH}	$\overline{OE}$	Y	1	4.9		6.2	1	3.4	4.7		6	ns
t_{PZL}			1.1	4.9		6.7	1.1	3.4	4.7		6.5	
t_{PHZ}	$\overline{OE}$	Y	1.8	5.3		5.9	1.8	3.7	5.1		5.7	ns
t_{PLZ}			1.3	4.7		4.2	1.3	2.6	4.5		4	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION
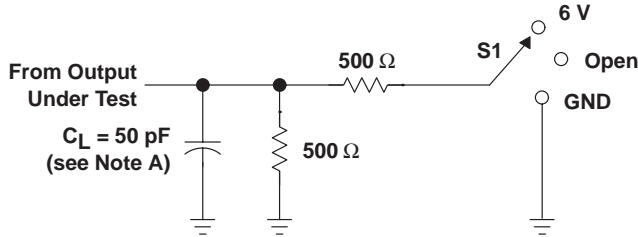
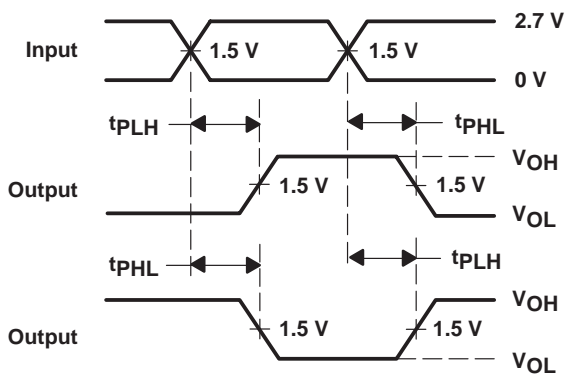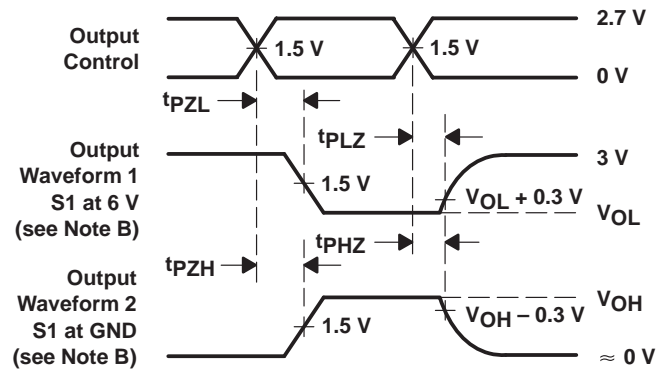| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT FOR OUTPUTS
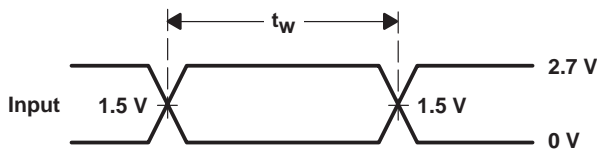
**VOLTAGE WAVEFORMS
PULSE DURATION**
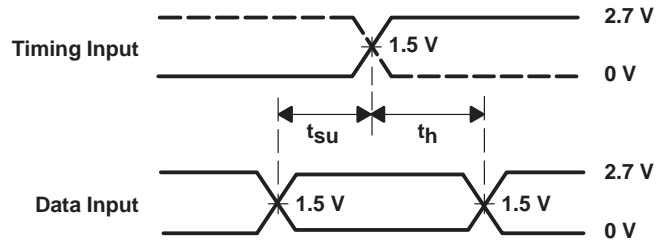
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PRODUCT SUPPORT: TRAINING

SN74LVT125, 3.3-V ABT Quadruple Bus Buffers With 3-State Outputs
DEVICE STATUS: **ACTIVE**

RECOMMENDED REPLACEMENT DEVICES

Part Number	Comments
SN74LVTH125	The device has the SAME FUNCTIONALITY and PINOUT as the compared device but is NOT an exact equivalent.Device Revision (PCN Number: PCN 5287C)

PARAMETER NAME	SN74LVT125
Voltage Nodes (V)	3.3, 2.7
Vcc range (V)	2.7 to 3.6
Input Level	TTL/CMOS
Output Level	LVTTL
Output Drive (mA)	-32/64
tpd max (ns)	4
Static Current	3.6

FEATURES   ▲Back to Top

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DESCRIPTION   ▲Back to Top

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DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74LVT125D	ACTIVE	SOP (D) | 14	-40 TO 85	View Contents	1KU | 0.91	50	5189	2550 | 23 Sep	4 WKS	Avnet | AMERICA	>1k	BUY NOW
								>10k | 14 Oct		DigiKey | AMERICA	619	BUY NOW
								>10k | 21 Oct				
SN74LVT125DBLE	OBSOLETE	SSOP (DB) | 14	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74LVT125DBR	ACTIVE	SSOP (DB) | 14	-40 TO 85	View Contents	1KU | 0.91	2000	N/A*	>10k | 21 Oct	4 WKS			
SN74LVT125DR	ACTIVE	SOP (D) | 14	-40 TO 85	View Contents	1KU | 0.95	2500	5000	1326 | 23 Sep	3 WKS	Avnet | AMERICA	>1k	BUY NOW
								3231 | 24 Sep		DigiKey | AMERICA	>1k	BUY NOW
								6030 | 25 Sep				
								>10k | 14 Oct				
								>10k | 17 Oct				
SN74LVT125NSR	ACTIVE	SOP (NS) | 14		View Contents	1KU | 0.98	2000	N/A*	>10k | 14 Oct	4 WKS			
								>10k | 21 Oct				
SN74LVT125PWLE	OBSOLETE	TSSOP (PW) | 14	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74LVT125PWR	ACTIVE	TSSOP (PW) | 14	-40 TO 85	View Contents	1KU | 0.90	2000	10k	2000 | 03 Oct	4 WKS	Avnet | AMERICA	>1k	BUY NOW
								>10k | 10 Oct		DigiKey | AMERICA	>1k	BUY NOW
								>10k | 17 Oct				
								8000 | 21 Oct				

Table Data Updated on: 9/26/2002