Features

- Typical propagation delay: 8ns
- Fan out of LS-TTL loads
- Quiescent power consumption: 10μW maximum at room temperature
- Low input current: 1μA maximum

Description

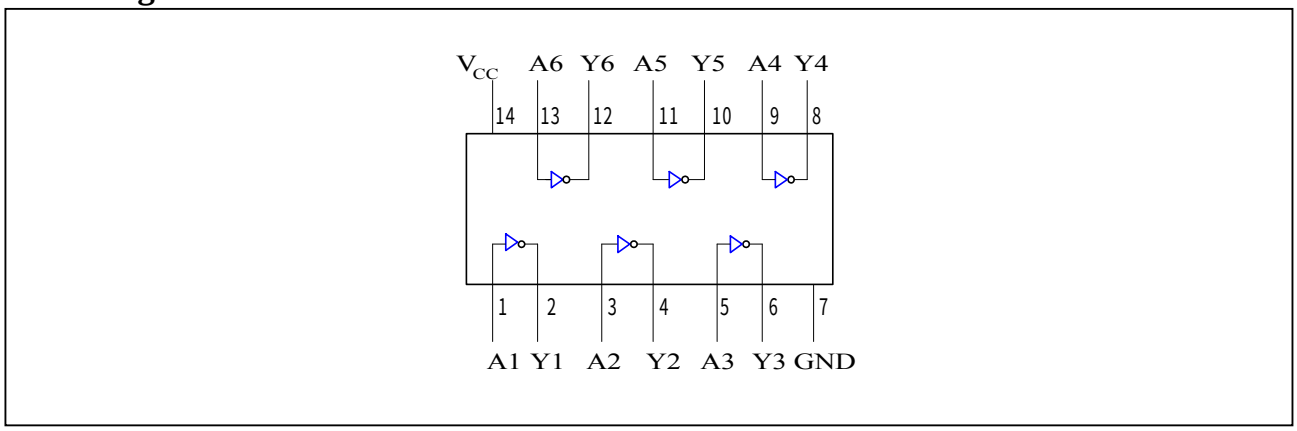
The PT74HC04 inverters utilize advanced silicon-gate CMOS technology to achieve operating speed similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits.

The PT74HC04 is a triple buffered inverter. It has high noise immunity and the ability to drive 10 LS-TTL loads. The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

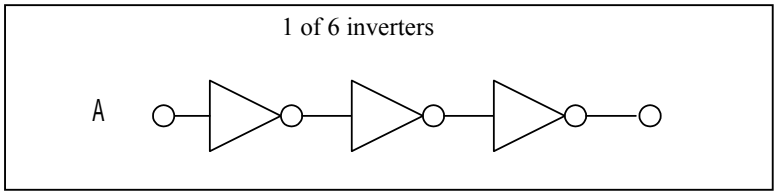
Ordering Information

Ordering No.	Package
PT74HC04W	SOIC-14
PT74HC04WE	Lead free SOIC-14
PT74HC04P	DIP-14
PT74HC04PE	Lead free DIP-14

Pin Configuration



Logic Diagram



Maximum Ratings

Ambient Temperature with Power Applied ..... -40°C to +85°C
Supply Voltage to Ground Potential (V_{CC} to GND) ..... -0.5V to 7.0V
DC Input Voltage (V_{IN}) ..... -1.5V to V_{CC}+1.5V
DC Output Voltage (V_{OUT}) ..... -0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK}) ..... ±20mA
DC Output Current, per pin (I_{OUT}) ..... ±25mA
DC V_{CC} or GND Current, per pin (I_{CC}) ..... ±50mA
Power Dissipation (P_D) * 600mW
S. O. Package only 500mV

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

* Power Dissipation temperature derating - plastic *PDIP* package: -12 mW/°C from 65°C to 85°C.

Recommended operation conditions

Sym	Description	Test Conditions	Min	Typ	Max	Unit
V_{cc}	Supply voltage	-	2.0	-	6.0	V
V_{IN}, V_{OUT}	DC input or output voltage	-	0.0	-	Vcc	V
T_A	Operating temperature	-	-40	-	85	℃
T_r, T_f	Input rise or fall time	Vcc=2.0V	-	-	1000	nS
		Vcc=4.5V	-	-	500	
		Vcc=6.0V	-	-	400	

DC Electrical Characteristics

Sym	Parameter	Test Conditions	V_{CC}	T_A=25℃	T_A= -40 to 85℃	T_A= -40 to 125℃	Unit
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	-	2.0V 4.5V 6.0V	- -	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum LOW Level Input Voltage	-	2.0V 4.5V 6.0V	- -	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} =V_{IH} or V_{IL} $\|I_{OUT}\| \le 20$ μA	2.0V 4.5V 6.0V	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN} =V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA $\|I_{OUT}\| \le 5.2$ mA	4.5V 6.0V	4.2 5.7	3.98 5.48	3.84 5.34	3.7 5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} $\|I_{OUT}\| \le 20$ μA	2.0V 4.5V 6.0V	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN} =V_{IH} $\|I_{OUT}\| \le 4.0$ mA $\|I_{OUT}\| \le 5.2$ mA	4.5V 6.0V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V
I_{IN}	Maximum Input Current	V_{IN} =V_{CC} or GND	6.0V	-	±1.0	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} =V_{CC} or GND I_{OUT} = 0 μA	6.0V	-	2.0	20	40	μA

AC Electrical Characteristics

(V_{CC}= 5V, T_A= 25^{0}C, C_L=15pF, t_r=t_f= 6nS, Unless otherwise noted.)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	-	8	15	nS

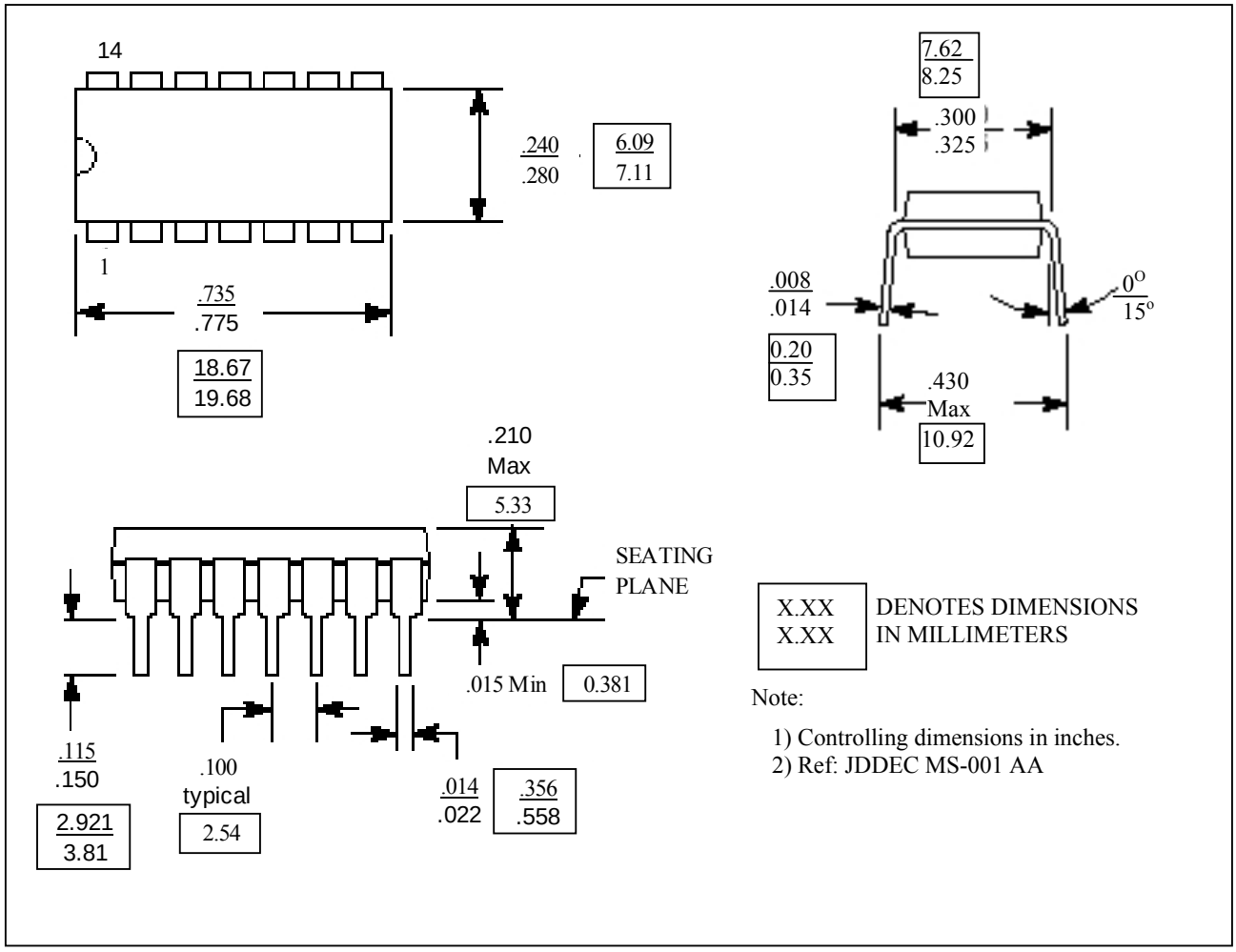
(V_{CC}=2.0V to 6.0V, C_L=50pF, tr=tf=6nS, Unless otherwise noted.)

Symbol	Parameter	Conditions	V_{CC}	T_A=25^{0}C	T_A= -40 to 85^{0}C	T_A= -40 to 125^{0}C		Units
				Typ	Guaranteed Limits			
t_{PHL} t_{PLH}	Maximum Propagation Delay	-	2.0V 4.5V 6.0V	55 11 9	95 19 16	120 24 20	145 29 24	nS
t_{THL} t_{TLH}	Maximum Output Rise and Fall Time	-	2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	nS
C_{PD}	Power Dissipation Capacitance(**Note**)	(per gate)	-	20	-	-	-	nS
C_{IN}	Maximum Input Capacitance	-	-	5	10	10	10	pF

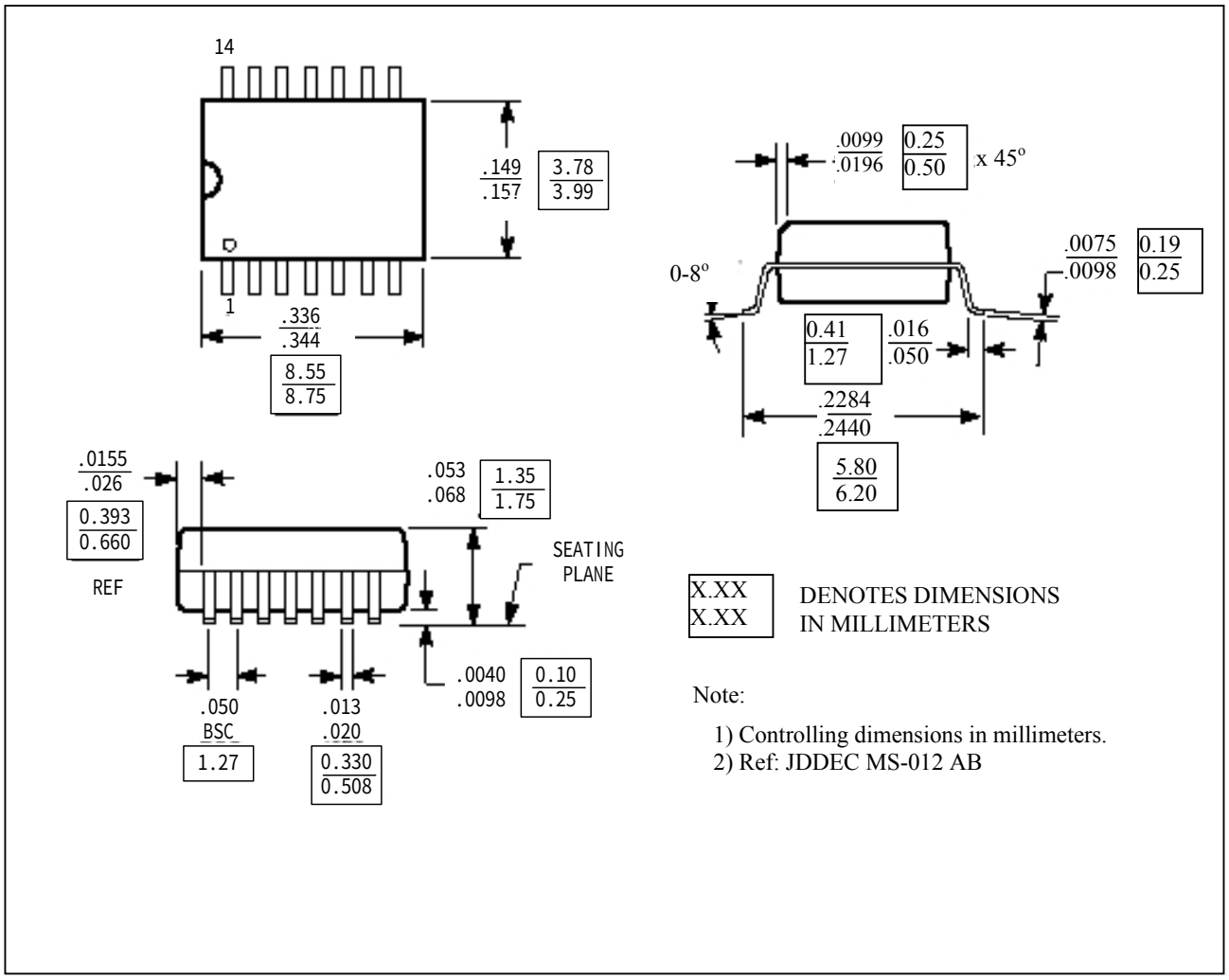
Note: C_{PD} determines the no load dynamic power consumption, P_D=$C_{PD}V_{CC}^2f$ + $I_{CC}V_{CC}$, and the no load dynamic current consumption. I_S= $C_{PD}V_{CC}f$ + I_{CC}.

Mechanical Information

P/PE (DIP-14)



W/WE (SOIC-14)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DENOTES DIMENSIONS
IN MILLIMETERS
Note:
1) Controlling dimensions in millimeters.
2) Ref: JDDEC MS-012 AB

Notes

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