

HARRIS SEMICOND SECTOR

58E D

T-43-21

CMOS NAND Gates

December 1992

Features

- High-Voltage Types (20V Rating)
- Propagation Delay Time = 60ns (typ.) at CL = 50pF, VDD = 10V
- Buffered Inputs and Outputs
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1 μ A at 18V Over Full Package-Temperature Range; 100nA at 18V and +25°C
- 100% Tested for Maximum Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Noise Margin (Over Full Package Temperature Range):
 - 1V at VDD = 5V
 - 2V at VDD = 10V
 - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standards No. 13B, "Standard Specifications for Description of "B" Series CMOS Device's

Description

CD4011BMS - Quad 2 Input

CD4012BMS - Dual 4 Input

CD4023BMS - Triple 3 Input

CD4011BMS, CD4012BMS, and CD4023BMS NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of CMOS gates. All inputs and outputs are buffered.

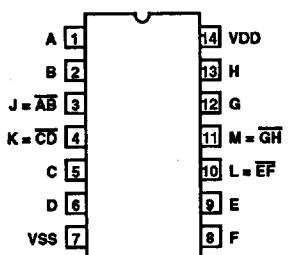
The CD4011BMS, CD4012BMS and the CD4023BMS is supplied in these 14 lead outline packages:

	CD4011B	CD4012B	CD4023B
Braze Seal DIP	H4Q	H4H	H4Q
Frit Seal DIP	H1B	H1B	H1B
Ceramic Flatpack	H3W	H3W	H3W

Pinouts

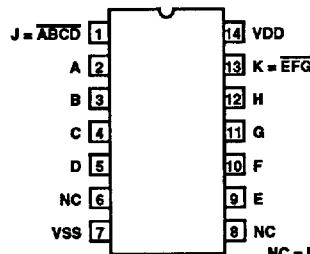
CD4011BMS

TOP VIEW



CD4012BMS

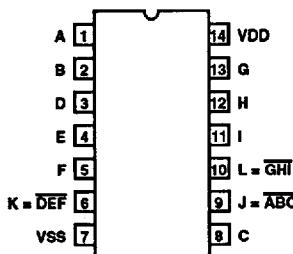
TOP VIEW



NC = NO CONNECTION

CD4023BMS

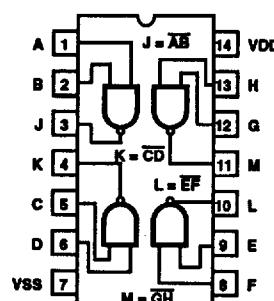
TOP VIEW



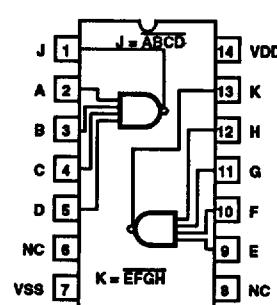
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LOGIC

Functional Diagrams

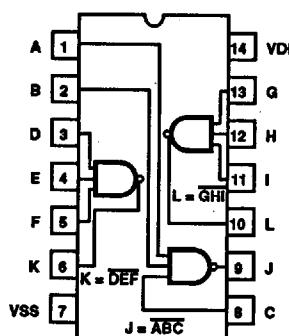


CD4011BMS



NC = NO CONNECTION

CD4012BMS



CD4023BMS

Specifications CD4011BMS, CD4012BMS, CD4023BMS**Absolute Maximum Ratings**

DC Supply Voltage Range, (VDD)	-0.5V to +20V
(Voltage Referenced to VSS Terminals)	
Input Voltage Range, All Inputs	-0.5V to VDD +0.5V
DC Input Current, Any One Input	±10mA
Operating Temperature Range.....	-55°C to +125°C
Package Types D, F, K, H	
Storage Temperature Range (TSTG).....	-65°C to +150°C
Lead Temperature (During Soldering)	+265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum	

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W
Maximum Package Power Dissipation (PD) at +125°C		
For TA = -55°C to +100°C (Package Type D, F, K)	500mW	
For TA = +100°C to +125°C (Package Type D, F, K)	Derate Linearity at 12mW/°C to 200mW	
Device Dissipation per Output Transistor	100mW	
For TA = Full Package Temperature Range (All Package Types)		
Junction Temperature		+175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1	+25°C	-	0.5	µA
			2	+125°C	-	50	µA
		VDD = 18V, VIN = VDD or GND	3	-55°C	-	0.5	µA
Input Leakage Current	IIL	VIN = VDD or GND	1	+25°C	-100	-	nA
			2	+125°C	-1000	-	nA
		VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	1	+25°C	-	100	nA
			2	+125°C	-	1000	nA
		VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load	1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)	1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V	1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND	7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND	7	+25°C			
		VDD = 18V, VIN = VDD or GND	8A	+125°C			
		VDD = 3V, VIN = VDD or GND	8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V	1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V	1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V	1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V	1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.

2. Go/No Go test with limits applied to inputs

3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	338	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	+55°C, +25°C	-	0.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	+55°C, +25°C	-	0.5	µA
				+125°C	-	15	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
				+25°C, +125°C, -55°C	-	50	mV
		VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
				+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	2.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

- NOTES: 1. All voltages referenced to device GND.
 2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

3. See Table 2 for +25°C limit.

4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	± 0.1µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	
Group A	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas
	Subgroup B-6	Sample 5005	1, 7, 9
Group D	Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2, 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

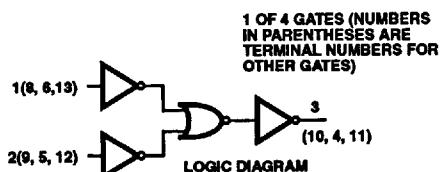
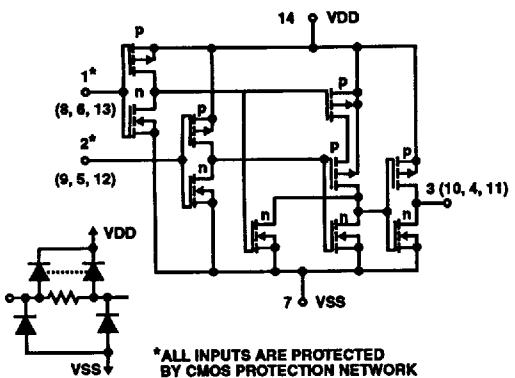
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V.	OSCILLATOR
					50kHz
					25kHz
PART NUMBER CD4011B					
Static Burn-In 1 Note 1	3, 4, 10, 11	1, 2, 5 - 9, 12, 13	14		
Static Burn-In 2 Note 1	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12 - 14		
Dynamic Burn-In Note 1	-	7	14	3, 4, 10, 11	1, 2, 5, 6, 8, 9, 12, 13
Irradiation Note 2	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12 - 14		
PART NUMBER CD4012B					
Static Burn-In 1 Note 1	1, 6, 8, 13	2 - 5, 7, 9 - 12	14		
Static Burn-In 2 Note 1	1, 6, 8, 13	7	2 - 5, 9 - 12, 14		
Dynamic Burn-In Note 1	6, 8	7	14	1, 13	2 - 5, 9 - 12
Irradiation Note 2	1, 6, 8, 13	7	2 - 5, 9 - 12, 14		
PART NUMBER CD4023B					
Static Burn-In 1 Note 1	6, 9, 10	1 - 5, 7, 8, 11 - 13	14		
Static Burn-In 2 Note 1	6, 9, 10	7	1 - 5, 8, 11 - 14		
Dynamic Burn-In Note 1	-	7	14	6, 9, 10	1 - 5, 8, 11 - 13
Irradiation Note 2	6, 9, 10	7	1 - 5, 8, 11 - 14		

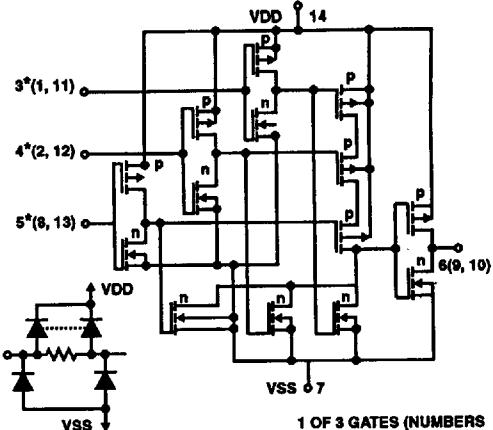
NOTE:

1. Each pin except VDD and GND will have a series resistor of $10K \pm 5\%$, VDD = $18V \pm 0.5V$
2. Each pin except VDD and GND will have a series resistor of $47K \pm 5\%$; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = $10V \pm 0.5V$

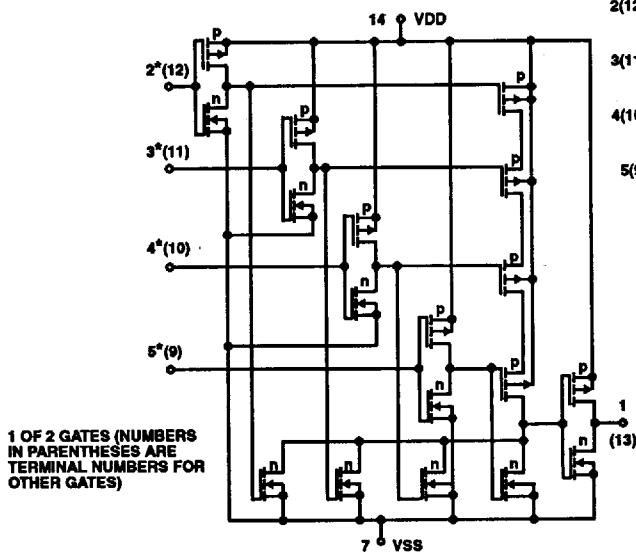
Schematic and Logic Diagrams



CD4011BMS



CD4023BMS



CD4012BMS

Typical Performance Characteristics

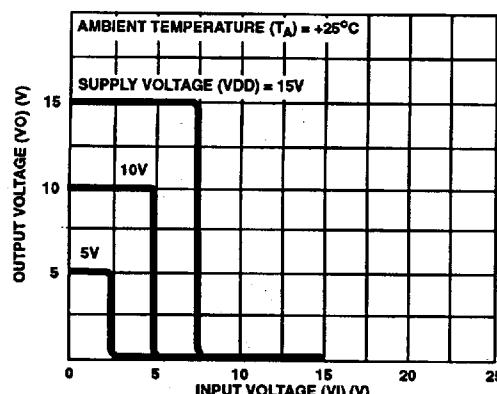


FIGURE 1. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS

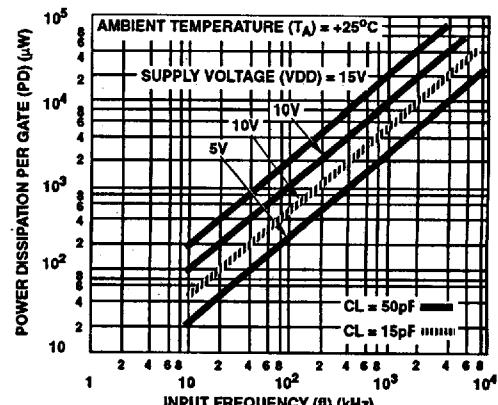


FIGURE 2. TYPICAL POWER DISSIPATION CHARACTERISTICS

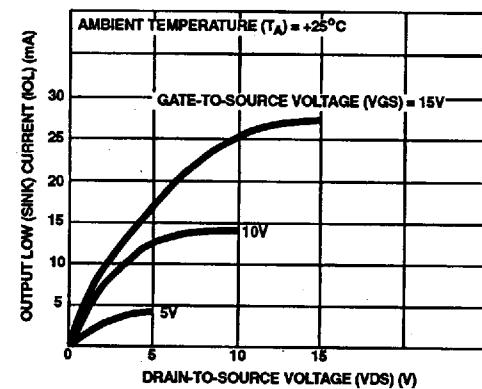


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

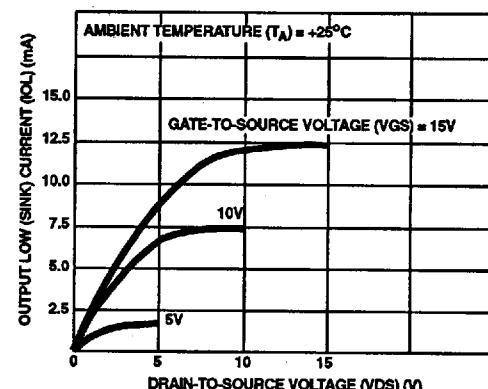


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

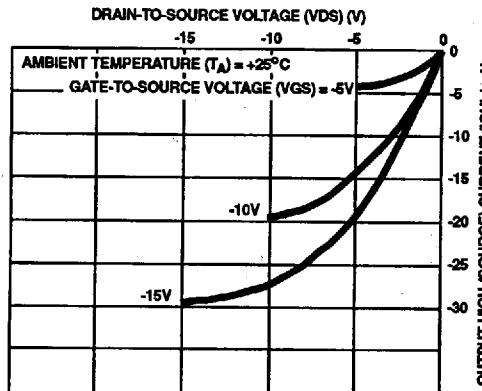


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

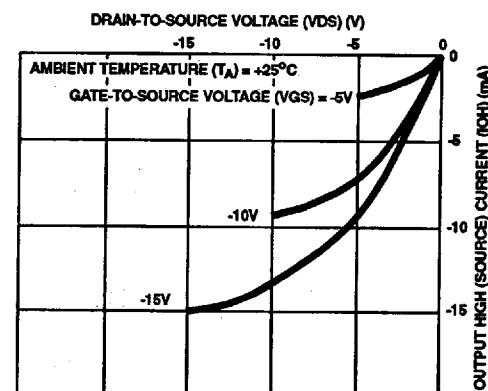


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

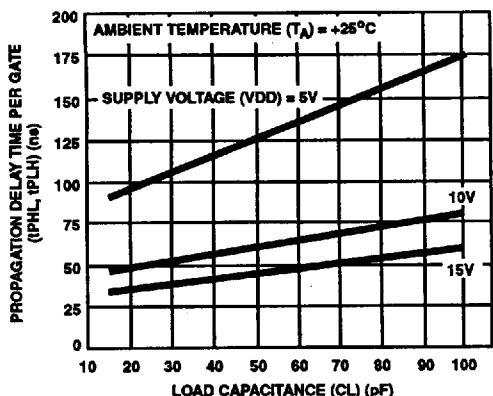


FIGURE 7. TYPICAL PROPAGATION DELAY TIME PER GATE AS A FUNCTION OF LOAD CAPACITANCE

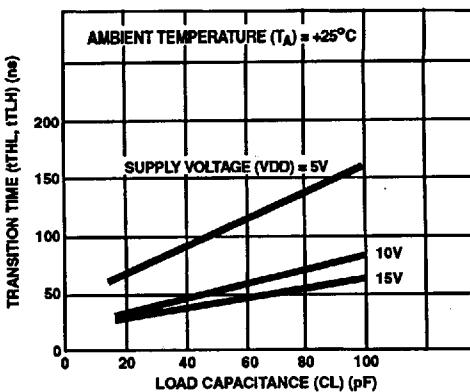
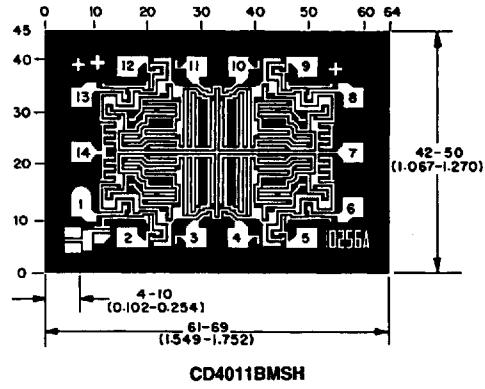
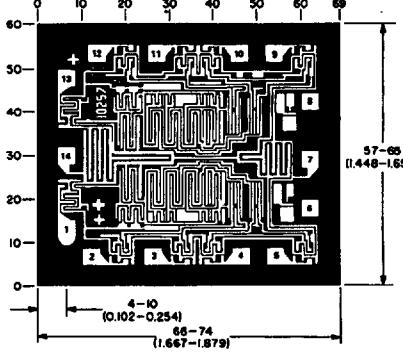


FIGURE 8. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

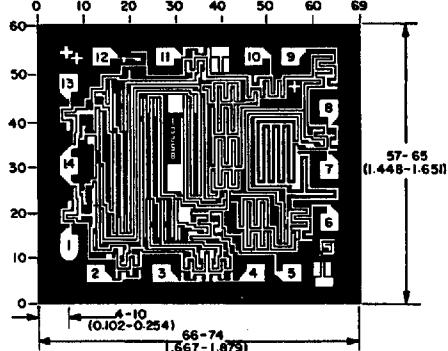
Chip Dimensions and Pad Layouts



CD4011BMS



CD4012BMS



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

CD4023BMS

7

LOGIC

METALLIZATION: Thickness: 11kÅ - 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches