MC54/74HCT533

Octal 3-State Inverting Transparent Latch with LSTTL-Compatible Inputs

High-Performance Silicon-Gate CMOS

The MC54/74HCT533 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

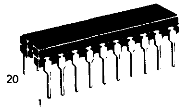
The HCT533 is identical in pinout to the LS533.

When Latch Enable is high, these latches appear transparent to data (i.e., the outputs change asynchronously). The data appears at the outputs in inverted form. When Latch Enable is taken low, data meeting the set-up and hold times becomes latched.

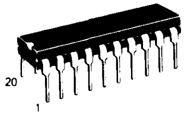
The Output Enable does not affect the state of the latch, but when Output Enable is high, all outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HCT533 is identical in function to the HCT563, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT373, which has noninverting outputs.

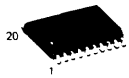
- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 256 FETs or 64 Equivalent Gates



J SUFFIX CERAMIC CASE 732-03



N SUFFIX PLASTIC CASE 738-03



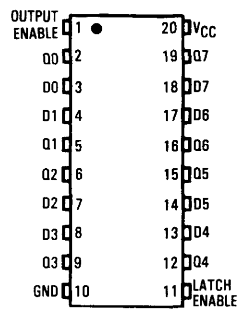
DW SUFFIX SOIC CASE 751D-03

ORDERING INFORMATION

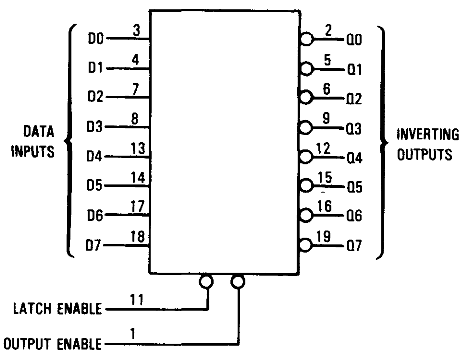
MC74HCTXXXN	Plastic
MC54HCTXXXJ	Ceramic
MC74HCTXXXDW	SOIC

T_A = −55° to 125°C for all packages.
Dimensions in Chapter 6.

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 20 = V_{CC}
PIN 10 = GND

FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	L
L	H	L	H
L	L	X	No Change
H	X	X	Z

X = don't care
Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	 260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	−55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in}=V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA	4.5	3.98	3.84	3.70	
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V_{in}=V_{IL} or V_{IH} V_{out}=V_{CC} or GND	5.5	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	5.5	8	80	160	μA

Symbol	Parameter	Test Conditions	V_{CC} V	≥ −55°C	25°C to 125°C	Unit
ΔI_{CC}	Additional Quiescent Supply Current	V_{in}=2.4 V, Any One Input V_{in}=V_{CC} or GND, Other Inputs I_{out}=0 μA	5.5	2.9	2.4	mA

NOTES:
1. Information on typical parametric values can be found in Chapter 4.
2. Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to −55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	35	44	53	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	35	44	53	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	35	44	53	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	35	44	53	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	65	pF

TIMING REQUIREMENTS (V_{CC} = 5.0 V ± 10%, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to −55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Input D to Latch Enable (Figure 4)	20	25	30	ns
t_h	Minimum Hold Time, Latch Enable to Input D (Figure 4)	5	6	8	ns
t_w	Minimum Pulse Width, Latch Enable (Figure 2)	16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

NOTE: Information on typical parametric values can be found in Chapter 4.

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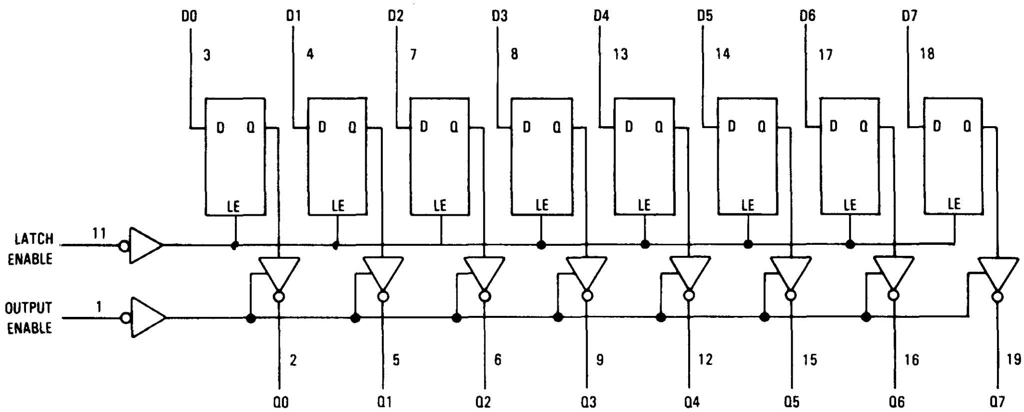
EXPANDED LOGIC DIAGRAM



SWITCHING WAVEFORMS

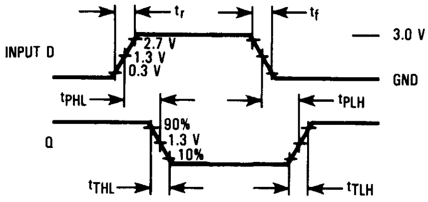


Figure 1.

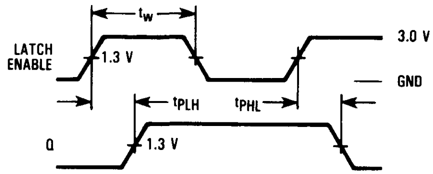


Figure 2.

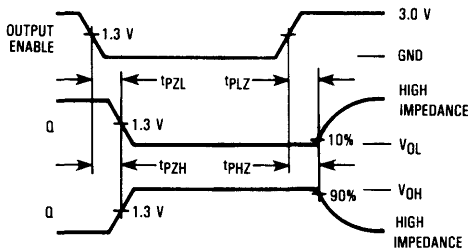


Figure 3.

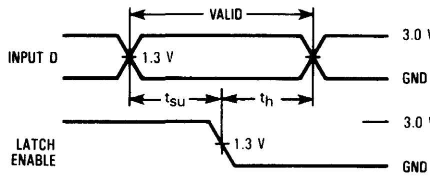
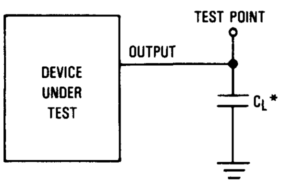


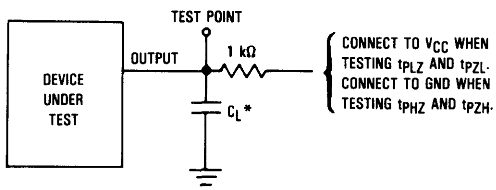
Figure 4.

TEST CIRCUITS



*Includes all probe and jig capacitance.

Figure 5.



* Includes all probe and jig capacitance.

Figure 6.