

# SN74LS640, SN74LS641, SN74LS642, SN74LS645

## Octal Bus Transceivers

These octal bus transceivers are designed for asynchronous two-way communication between data buses. Control function implementation minimizes external timing requirements. These circuits allow data transmission from the A bus to B or from the B bus to A bus depending upon the logic level of the direction control (DIR) input. Enable input ( $\bar{G}$ ) can disable the device so that the buses are effectively isolated.

DEVICE	OUTPUT	LOGIC
LS640	3-State	Inverting
LS641	Open-Collector	True
LS642	Open-Collector	Inverting
LS645	3-State	True

FUNCTION TABLE

CONTROL INPUTS		OPERATION	
		LS640 LS642	LS641 LS645
$\bar{G}$	DIR		
L	L	$\bar{B}$ data to A bus	B data to A bus
L	H	$\bar{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

H = HIGH Level, L = LOW Level, X = Irrelevant

### GUARANTEED OPERATING RANGES (SN74LS640, SN74LS645)

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-3.0	mA
				-15	mA
$I_{OL}$	Output Current – Low			24	mA

### GUARANTEED OPERATING RANGES (SN74LS641, SN74LS642)

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$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$V_{OH}$	Output Voltage – High			5.5	V
$I_{OL}$	Output Current – Low			24	mA

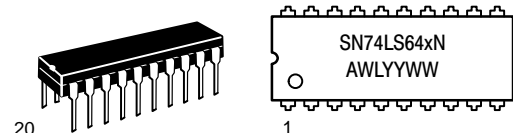


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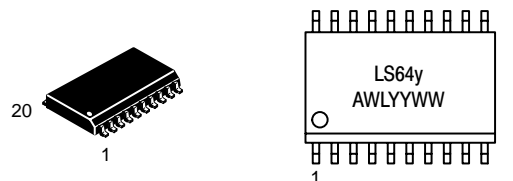
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## LOW POWER SCHOTTKY

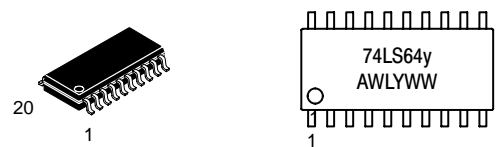
### MARKING DIAGRAMS



PDIP-20  
N SUFFIX  
CASE 738



SOIC-20  
DW SUFFIX  
CASE 751D



SOEIAJ-20  
M SUFFIX  
CASE 967

x = 0, 1, 2, or 5  
y = 0, 1, or 2  
A = Assembly Location  
WL = Wafer Lot  
Y, YY = Year  
WW = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

CONNECTION DIAGRAMS DIP (TOP VIEW)

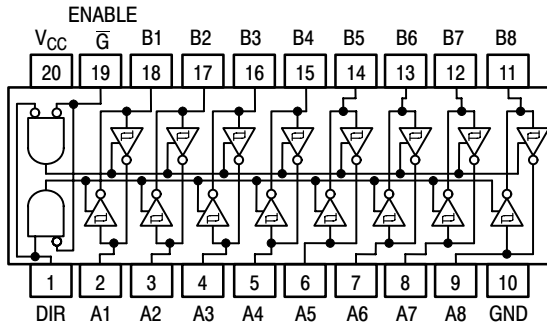


Figure 1. SN74LS640  
SN74LS642

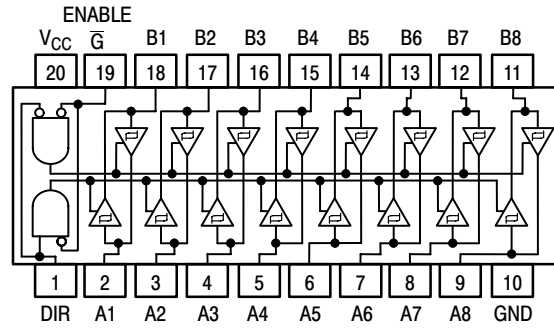


Figure 2. SN74LS641  
SN74LS645

## SN74LS640 • SN74LS645

### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.6	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4	3.4		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = 3.0 mA
		2.0			V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 12 mA
			0.35	0.5	V	I <sub>OL</sub> = 24 mA
I <sub>OZH</sub>	Output Off Current HIGH			20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V
I <sub>OZL</sub>	Output Off Current LOW			-400	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V
I <sub>IH</sub>	Input HIGH Current	A or B, DIR or $\bar{G}$		20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
		DIR or $\bar{G}$		0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
		A or B		0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 5.5 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Output Short Circuit Current (Note 1)	-40		-225	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current					
	Total Output HIGH			70	mA	V <sub>CC</sub> = MAX
	Total, Output LOW			90		
Total at HIGH Z			95			

1. Not more than one output should be shorted at a time, nor for more than 1 second.

### AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS640			LS645				
		Min	Typ	Max	Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A to B		6.0	10		8.0	15	ns	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω
			8.0	15		11	15		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay B to A		6.0	10		8.0	15		
			8.0	15		11	15		
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time $\bar{G}$ , DIR to A		31	40		31	40		
			23	40		26	40		
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time $\bar{G}$ , DIR to B		31	40		31	40		
			23	40		26	40		
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time $\bar{G}$ , DIR to A		15	25		15	25	ns	C <sub>L</sub> = 5.0 pF
			15	25		15	25		
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time $\bar{G}$ , DIR to B		15	25		15	25		
			15	25		15	25		

## SN74LS641 • SN74LS642

### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.6	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
I <sub>OH</sub>	Output HIGH Current			100	μA	V <sub>CC</sub> = MIN, V <sub>OH</sub> = MAX
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 12 mA
			0.35	0.5	V	I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				-0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>CC</sub>	Power Supply Current Total, Output HIGH			70	mA	V <sub>CC</sub> = MAX
	Total, Output LOW			90		
	Total at HIGH Z			95		

### AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS641			LS642				
		Min	Typ	Max	Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, A to B		17 16	25 25		19 14	25 25	ns	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, B to A		17 16	25 25		19 14	25 25	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, $\overline{G}$ , DIR to A		23 34	40 50		26 43	40 60	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, $\overline{G}$ , DIR to B		25 37	40 50		28 39	40 60	ns	

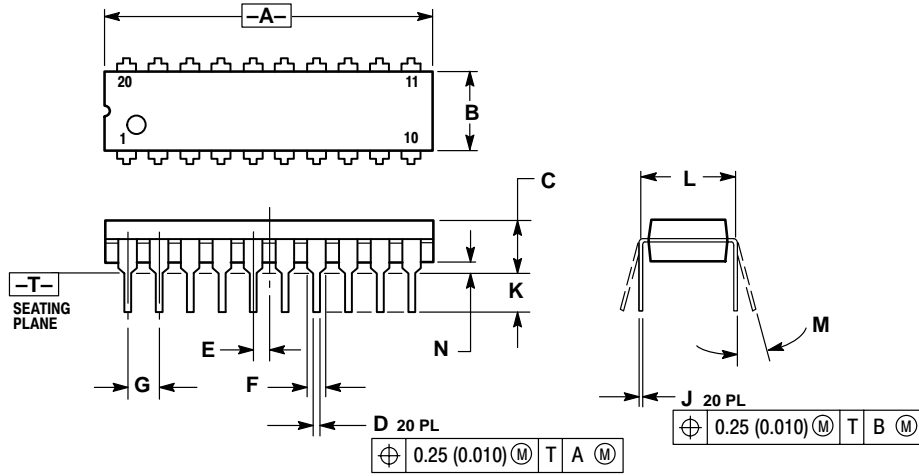
**DEVICE ORDERING INFORMATION**

<b>Device Order Number</b>	<b>Package Type</b>	<b>Tape and Reel Size</b>
SN74LS640N	PDIP-20	1440 Units/Box
SN74LS640DW	SOIC-WIDE	2500/Tape and Reel
SN74LS640DWR2	SOIC-WIDE	2500/Tape and Reel
SN74LS640M	SOEIAJ-20	See Note 2
SN74LS640MEL	SOEIAJ-20	See Note 2
SN74LS641N	PDIP-20	1440 Units/Box
SN74LS641DW	SOIC-WIDE	2500/Tape and Reel
SN74LS641DWR2	SOIC-WIDE	2500/Tape and Reel
SN74LS641M	SOEIAJ-20	See Note 2
SN74LS641MEL	SOEIAJ-20	See Note 2
SN74LS642N	PDIP-20	1440 Units/Box
SN74LS642DW	SOIC-WIDE	2500/Tape and Reel
SN74LS642DWR2	SOIC-WIDE	2500/Tape and Reel
SN74LS642M	SOEIAJ-20	See Note 2
SN74LS642MEL	SOEIAJ-20	See Note 2
SN74LS640N	PDIP-20	1440 Units/Box

2. For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

# PACKAGE DIMENSIONS

## N SUFFIX PLASTIC PACKAGE CASE 738-03 ISSUE E



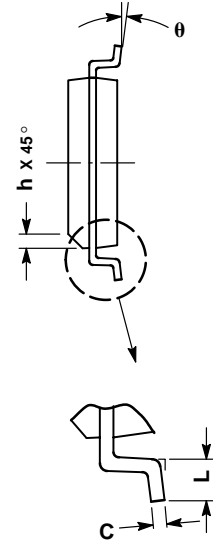
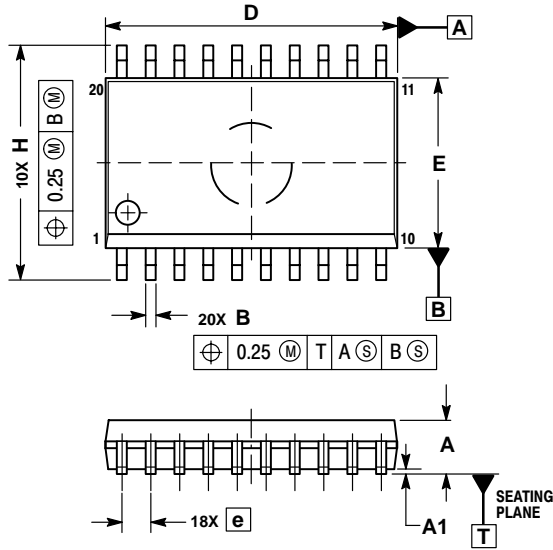
### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

# PACKAGE DIMENSIONS


## D SUFFIX PLASTIC SOIC PACKAGE CASE 751D-05 ISSUE F



**NOTES:**

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
$\theta$	$0^\circ$	$7^\circ$

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