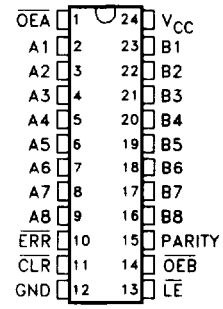
SN74BCT29853, SN74BCT29854
8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

D3031, SEPTEMBER 1987—REVISED JULY 1989

- **BiCMOS Process with TTL Inputs and Outputs**
- **BiCMOS Design Reduces Standby Current**
- **Flow-Through Pinout (All Inputs on Opposite Side from Outputs)**
- **Functionally Equivalent to AMD Am29853 and Am29854**
- **High-Speed Bus Transceivers with Parity Generator/Checker**
- **Parity Error Flag with Open-Collector Output**
- **Choice of True ('BCT29853) or Inverting ('BCT29854) Logic**
- **Has a Latch for Storage of the Parity Error Flag**
- **Package Options Include Plastic "Small Outline" Package, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74BCT' ... DW OR NT PACKAGE
(TOP VIEW)



description

The SN74BCT29853 and SN74BCT29854 are 8-bit to 9-bit parity transceivers designed for two-way communication between data buses. When data is transmitted from the A to B bus, a parity bit is generated. When data is transmitted from the B to A bus with its corresponding parity bit, the $\overline{ERR}$ output will indicate whether or not an error in the B data has occurred. The output enable inputs $\overline{OEA}$ and $\overline{OEB}$ can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd output (PARITY), and monitors the parity of the I/O ports with an open-collector parity error flag ($\overline{ERR}$). $\overline{ERR}$ can be either passed, sampled, stored, or cleared from the latch using the $\overline{LE}$ and $\overline{CLR}$ control inputs. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The SN74BCT29853 and SN74BCT29854 are characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
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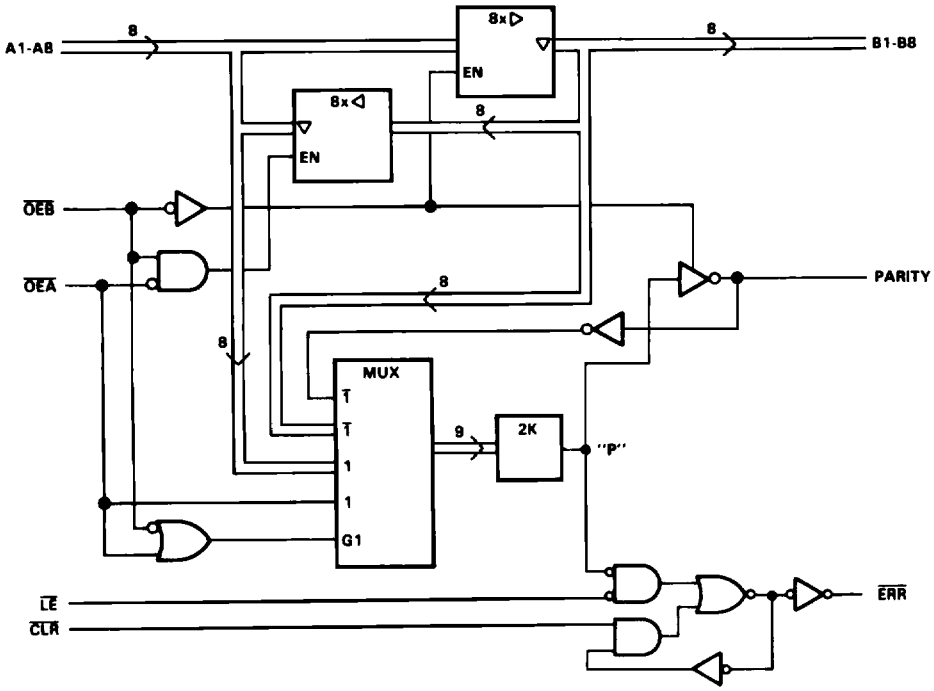
logic diagram (positive logic)

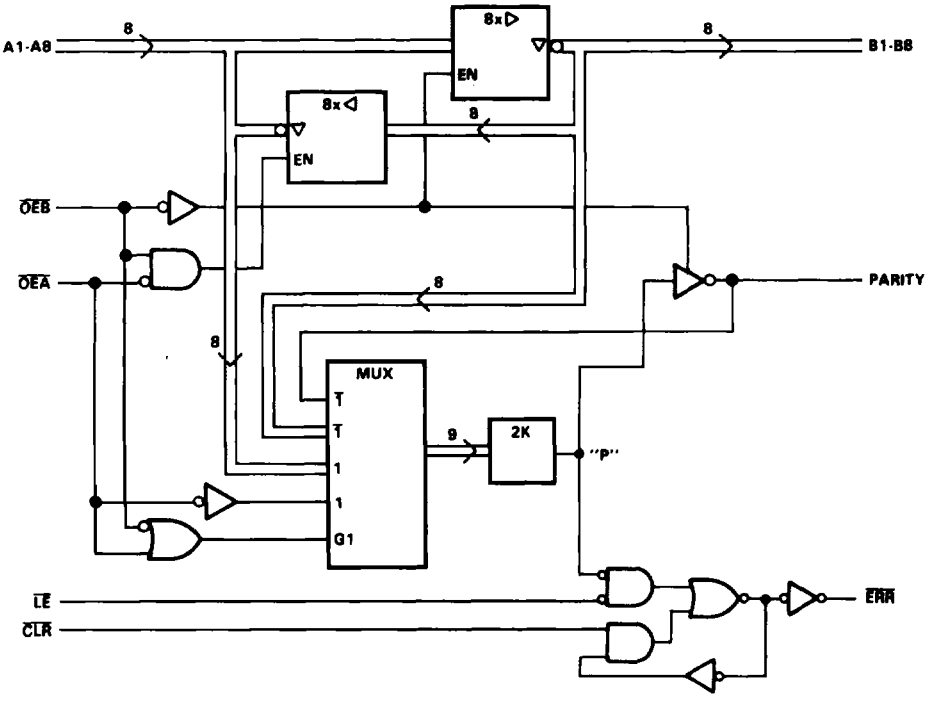


FUNCTION TABLE

INPUTS						OUTPUT & I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	$\overline{LE}$	Ai Σ of H's	Bi† Σ of H's	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A Data to B Bus and Generate Parity
H	L	X	L	NA	Odd Even	B	NA	NA	H L	B Data to A Bus and Check Parity
H	L	H	H	NA	X	X	NA	NA	N-1	Store Error Flag
X	X	L	H	X	X	X	NA	NA	H	Clear Error Flag Register
H	H	H L X X	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H H L	Isolation§ (Parity Check)
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care
†Summation of high-level inputs includes PARITY along with Bi inputs.
‡Output states shown assume the $\overline{ERR}$ output was previously high.
§In this mode the $\overline{ERR}$ output, when enabled, shows inverted parity of the A bus.

logic diagram (positive logic)



FUNCTION TABLE

INPUTS						OUTPUT & I/O				
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	$\overline{LE}$	AI Σ of H's	BI† Σ of L's	A	B	PARITY	$\overline{ERR}$‡	FUNCTION
L	H	X	X	Odd Even	NA	NA	$\overline{A}$	H L	NA	$\overline{A}$ Data to B Bus and Generate Parity
H	L	X	L	NA	Odd Even	$\overline{B}$	NA	NA	H L	$\overline{B}$ Data to A Bus and Check Parity
H	L	H	H	NA	X	X	NA	NA	N-1	Store Error Flag
X	X	L	H	X	X	X	NA	NA	H	Clear Error Flag Register
H	H	H L X X	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H L H	Isolation§
L	L	X	X	Odd Even	NA	NA	$\overline{A}$	L H	NA	$\overline{A}$ Data to B Bus and Generate Inverted Parity

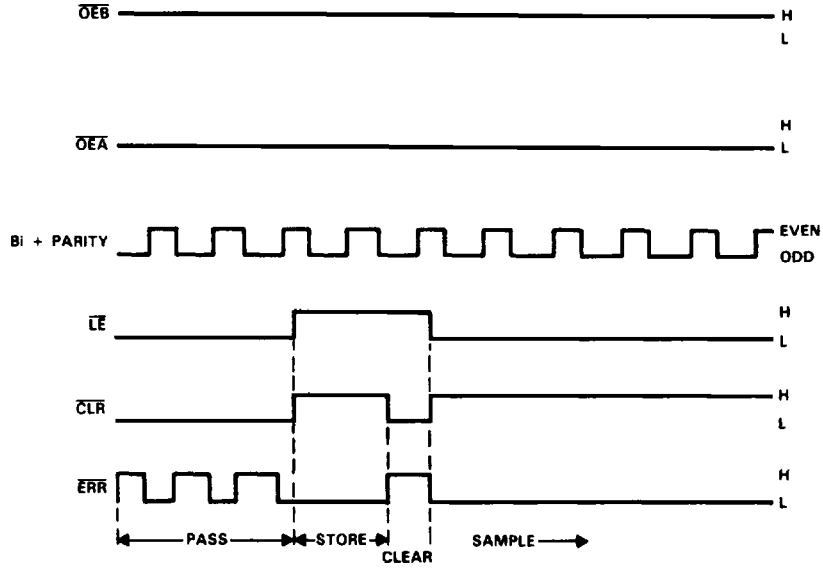
NA = Not applicable, NC = No change, X = Don't care

†Summation of low-level inputs includes PARITY along with Bi inputs.

‡Output states shown assume the $\overline{ERR}$ output was previously high.

§In this mode the $\overline{ERR}$ output, when enabled, shows noninverted parity of the A bus.

error flag waveforms



ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
$\overline{LE}$	$\overline{CLR}$	POINT "P"	$\overline{ERR}_{n-1}$†	$\overline{ERR}$	
L	L	L H	X	L H	PASS
L	H	L X H	X L H	L L H	SAMPLE
H	L	X	X	H	CLEAR
H	H	X	L H	L H	STORE

†ERR_{n-1} represents the state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, $\overline{LE}$ or point P.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage ..... 7 V
Voltage applied to a disabled I/O port ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage, $\overline{ERR}$				2.4	V
I_{OH}	High-level output current				−24	mA
I_{OL}	Low-level output current				48	mA
t_w	Pulse duration	$\overline{LE}$ low	10			ns
		$\overline{CLR}$ low	10			
t_{su}	Setup time before $\overline{LE}\downarrow$	Bi and PARITY	12			ns
t_h	Hold time, Bi and PARITY after $\overline{LE}\downarrow$		3			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	All inputs/outputs except $\overline{ERR}$	V_{CC} = 4.5 V	I_{OH} = −15 mA	2.4			V
			I_{OH} = −24 mA	2			
I_{OH}	$\overline{ERR}$	V_{CC} = 4.5 V,	V_{OH} = 2.4 V			20	μA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}‡	Data	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
	Control					−0.75	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−75		−250	mA
I_{CCL}		V_{CC} = 5.5 V,	All outputs open		55	80	mA
I_{CCZ}					30	45	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters include off-state output current for I/O ports only.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed 1 second.

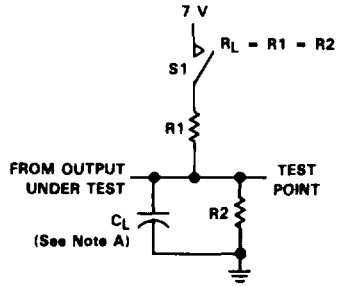
SN74BCT29853 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	5	7	1	10	ns
t_{PHL}			1	5	7	1	10	
t_{PLH}	A	PARITY	1.5	10	13	1.5	15	ns
t_{PHL}			1.5	10	13	1.5	15	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	13	16	2	20	ns
t_{PZL}			2	13	16	2	20	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	13	16	2	20	ns
t_{PLZ}			2	13	16	2	20	
t_{PHL}	$\overline{LE}$	$\overline{ERR}$	1.5	5	7	1.5	9	ns
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	1.5	11	14	1.5	15	ns
t_{PLH}	$\overline{OEA}$	PARITY	1.5	10	13	1.5	15	ns
t_{PHL}			1.5	10	13	1.5	15	
t_{PLH}	Bi/PARITY	$\overline{ERR}$	1.5	17	22	1.5	24	ns
t_{PHL}			1.5	10	13	1.5	16	

SN74BCT29854 switching characteristics (see Figure 1)

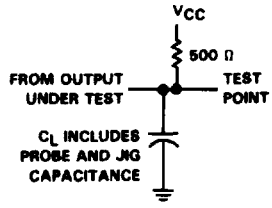
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	5	7	1	8	ns
t_{PHL}			1	5	7	1	8	
t_{PLH}	A	PARITY	1.5	10	13	1.5	15	ns
t_{PHL}			1.5	10	13	1.5	15	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	12	15	2	17	ns
t_{PZL}			2	13	16	2	19	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	8	11	2	15	ns
t_{PLZ}			2	10	14	2	17	
t_{PHL}	$\overline{LE}$	$\overline{ERR}$	1.5	5	7	1.5	9	ns
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	1.5	11	13	1.5	15	ns
t_{PLH}	$\overline{OEA}$	PARITY	1.5	10	13	1.5	15	ns
t_{PHL}			1.5	10	13	1.5	16	
t_{PLH}	Bi/PARITY	$\overline{ERR}$	1.5	15	18	1.5	20	ns
t_{PHL}			1.5	10	13	1.5	15	

PARAMETER MEASUREMENT INFORMATION

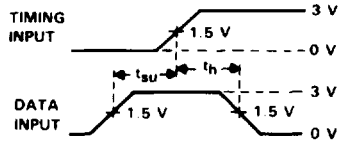


SWITCH POSITION TABLE

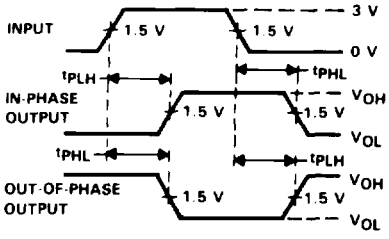
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



LOAD CIRCUIT 1 ALL OUTPUTS EXCEPT FOR ERROR FLAG

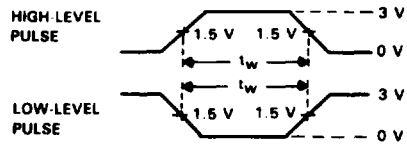


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

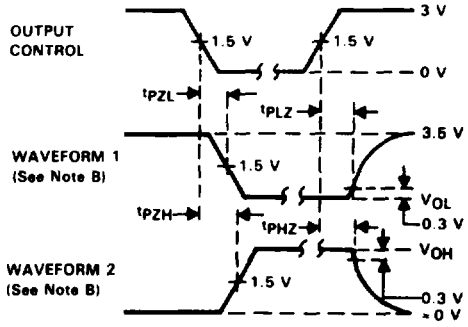


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

LOAD CIRCUIT 2 ERROR FLAG OUTPUT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1